A Flexible Scheme for Adaptive Integration Time Control

Andreas Breidenassel, Karlheinz Meier, Johannes Schemmel

Kirchhoff-Institute for Physics, University of Heidelberg
Im Neuenheimer Feld 227, 69120 Heidelberg, Germany
E-mail: breiden@kip.uni-heidelberg.de

Abstract

A scheme to regulate the integration time in an array of charge integrators in dependence of the individual discharging rate is presented. The regulation scheme can be used for the design of high dynamic range imagers. It has been implemented in a prototype imager realized in a standard 0.25 μm CMOS technology offering a resolution of 170 x 170 pixels with a pitch of 7.5 μm. A movable window allows the selection of the region of interest where high dynamic range capability is desired. Experimental results show a dynamic range of 135 dB.

Keywords

CMOS imager, high dynamic range, APS

INTRODUCTION

The natural world exhibits a vast range of light intensities spanning approximately 9 orders of magnitude from bright sunlight down to star-lit scenes. The human eye, equipped with the ability to adapt to the predominant intensity is capable to cover nearly the whole scale of occurring intensities[1]. In contrast to the eye, the dynamic range of artificial image sensors is often not wide enough to cover the dynamic range of the perceived scene, which results in a lost of information. Conventional CCD[2] imagers, typically offering a dynamic range of 65-75 dB, are incapable to cope with high dynamic range (HDR) situations. CMOS technology offers the opportunity to implement HDR sensors, which are able to capture scenes in which the light intensity varies over several orders of magnitude.

Several approaches to build HDR imagers have been explored so far. The different concepts range from sensors with logarithmic response [1] or capacity adjusting schemes [2] to global or local multiple sampling techniques and others [3–6]. Many implementations explored so far suffer from a reduced signal-to-noise ratio or big pixel pitches resulting from a complex pixel circuitry. Another problem is the potentially complex image reconstruction from the recorded data. Theoretical analysis of different schemes suggests an advantage of multiple sampling based concepts with respect to SNR in comparison to other concepts [7]. But even multiple sampling concepts differ strongly with respect to pixel size and necessary effort to reconstruct the final image. The presented implementation addresses some of these problems and realizes an HDR imager of diverse applicability. It was build to be used as an optical input channel for an artificial

---

[1]Thereof approximatly 4 decades in a single view.
[2]Charge Coupled Device

neural network. A movable HDR window, which should be controlled by the neural network, makes it possible to dynamically select regions of interest that provide information spanning several decades of light intensity.

CONTROL SCHEME

Regulation of the integration time is one of different possibilities to keep an integrating pixel from saturation, i.e. to keep its output voltage within a certain valid range ($V_{sig} > V_{sat}$). A scheme to regulate the integration time T_{int} should fulfill certain requirements to be useful: First, it should work locally i.e. adapt T_{int} individually for every pixel instead of taking many frames at different T_{int}. The latter would lead to a high storage demand for the data of multiple frames, a complex image reconstruction and a smaller frame rate than possible. Second, the scheme should be able to regulate T_{int} in multiple steps instead of applying a simple dual sampling, which would result in a significant dip in SNR [7]. Third, a sequential readout of complete rows in parallel to the corresponding HDR information should be possible to permit easy post-processing and interfacing. Furthermore, it would be desirable to have the regulation electronics outside of the pixel to avoid sacrificing resolution.

To fulfill these requirements, a regulation as shown in Fig. 1 is proposed: The necessary adaptive control of the integration
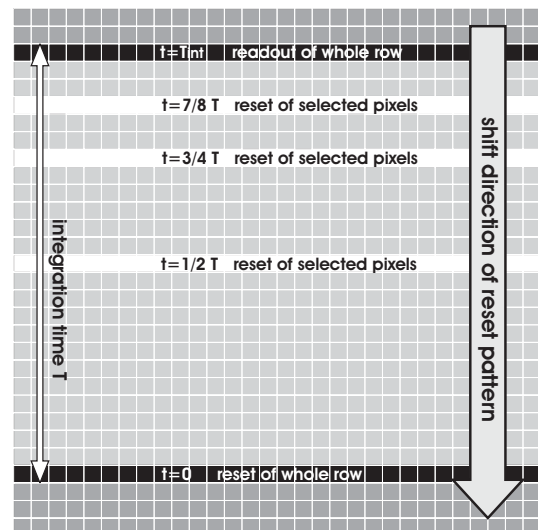

Figure 1. *Global schedule of the regulation scheme.*

time is realized by a sequential time series of charge resets on individual pixels. The scheme can be thought as a fixed

pattern of "reset curtains" that is shifted over the pixel array with constant speed.

The reset curtains follow each other with exponentially decreasing distance in time. Shown is the simple case of three regulation steps with a factor of 2 in time between two successive curtains. In every curtain the reset conditions are tested for every pixel of the selected row. Two conditions must be fulfilled for a reset of a single pixel of this row: First, the voltage at the readout amplifier of the pixel (V_{sig}) must decrease below half of the voltage range of the pixel. Second, the pixel must have been reset in the previous reset curtain.

By this scheme it is guaranteed that at the end of the longest possible integration time T_{max} all pixels of the selected row of the pattern (top black row in Fig. 1) have valid values and the whole row can be read out. To reconstruct the true intensity at a particular pixel location, it is necessary to know the integration time of that pixel, i.e. in which reset curtain it has been reset. For this reason, every time a pixel is reset, a time stamp is stored in a local memory to indicate the corresponding reset curtain. Image reconstruction is very easy because the sampled analog value of a pixel only has to be multiplied by the individual integration time which is equivalent to a bit shift of the digitized analog value by the recorded exponent of the integration time. This could be easily integrated on chip.

Accordingly to the pending tasks, the row accesses shown in Fig. 1 can be divided into two different types: During the first one (white rows in Fig. 1), in the following named as HDRcycle, the two reset conditions have to be tested, a reset of individual pixels where both conditions are fulfilled has to be done and the corresponding time stamps have to be stored. During the second one (black rows), in the following named as DScycle, the final analog integration results will be read out using double sampling (see next section). Afterwards the whole row is reset.

The finite duration of these cycles leads to a problem for the selection of the row which has to be accessed next, i.e. the row sequence. On the one side, it has to be guaranteed that the distance of the reset curtains have an exponentially decreasing distance in time for every row. On the other side the number of reset curtains and the number of rows of the sensor define how many (non overlapping) row accesses have to be made within the given integration time T_{max} (here: $16 \cdot 170 = 2270$ within 33 ms). A distribution of row accesses over T_{max} which fulfills these criteria has to be found by simulation. Additionally a calculation of the next row number to be accessed should be possible instead of relying on a huge lookup table that would grow in size with an increasing imager resolution.

The regulation scheme allows the implementation of an HDR "window mode". Here, a movable window of predefined size makes it possible to dynamically select regions of interest that provide HDR. This is possible by leaving out the HDRcycles for rows outside of the window and restricting the possible

reset to the predefined region for rows that are located inside the window. The window is especially useful for the realization of high resolution imagers if it is not necessary to instantaneously provide HDR information of the whole sensor array. A strong reduction of the size of the local memory which is necessary to hold the time stamps can be reached by this way. Furthermore the HDR information can also be used in conjunction with averaging of pixels. This results in HDR over the whole array in a single frame at the price of a reduced resolution.

SYSTEM ARCHITECTURE

Fig. 2 shows a photomicrograph of the sensor chip. Build in a $0.25\,\mu m$ CMOS (3 metal, 1 poly) process the chip size is 2 mm x 4 mm. Logically the chip can be divided into three blocks: The sensor itself, the regulation block for the high dynamic range expansion (HDRunit) and the double sampling unit (DSunit) where the analog data acquisition is done.

The dominating part of the chip is made up by the 170x170 pixel array. Fig. 3 shows a circuit diagram of a single pixel. It consists of an APS[3] with a n^+-diffusion diode as light sensing element, together with the circuitry for signal averaging with the next neighbors and for an individual reset. Averaging is possible for 2x2, 4x4 or 8x8 pixels over the whole sensor array. Apart from the pixels itself the sensor block also hosts the address decoders and drivers for the selection of individual rows and the logic for the selection of the desired averaging scheme.
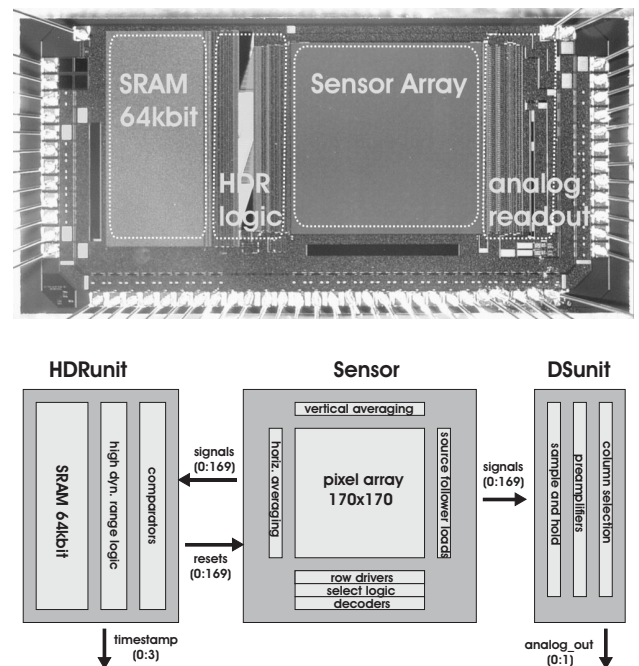
Figure 2. *Chip photomicrograph and corresponding block diagram. The chip size is 2 mm x 4 mm.*

---

[3]Active Pixel Sensor
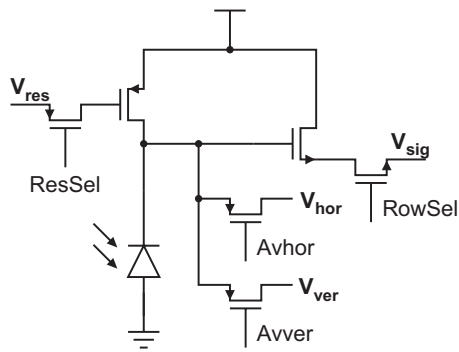
Figure 3. *Circuit diagram of the pixel.*

The second largest block on the chip is made up by a 64 kbit SRAM. As part of the HDRunit this memory is used to store the individual integration times of every pixel. Since the integration time is regulated in exponential steps with a constant basis it is only necessary to store the exponent of the regulation factor for a single pixel to be able to reconstruct the integration time. The size of this time stamp depends upon the max. number of reset curtains that will be used. In the presented implementation a stamp size of 4 bit was chosen permitting 16 reset curtains. Therefore the size of the SRAM is sufficient for a HDR window of 128 x 128 pixels. The SRAM and the pixel matrix are connected with each other by the HDR logic, where the conditions for a reset are tested individually for every pixel of the selected row. The analog signals of the selected row coming from the pixel array are connected to latched comparators to be compared with a reference voltage to determine if the first condition for the reset is fulfilled. At the same time the corresponding time stamp that is read back by the sense amplifiers from the SRAM delivers the information if the pixel has been reset in the previous reset cycle (2. reset condition). If both conditions are true for a particular pixel, it will be reset via its individual reset line and the new time stamp will be stored (HDRcycle). In case of a DScycle the final time stamps that were read from SRAM are copied to a shift register to sequentially read out the integration time information in parallel to the sequential analog readout. Furthermore the HDRunit takes care of the mapping and rearrangement of the data taken from the selectable HDR window position to be stored in SRAM. This has to be done also for the different modes of averaging. The whole HDRunit is capable to process a window of 128 x 128 pixels, but in the present prototype sensor implementation only a window of 85 x 85 is used.

The third block of the chip, the double sampling unit, consists of the sample and hold stages for the analog data acquisition, circuitry for the sequential data read out and the off chip drivers. The operating procedure follows the known method of double sampling to remove the pixel FPN: The signal voltages of a row that has finished integration are sampled during the DScycle onto a bank of PMOS capacitors (1 pF).

Subsequently the whole row will be reset and these reset values are sampled onto a second capacitor bank. In the current implementation a DScycle takes $1.8\,\mu$s whereas an HDRcycle takes 800 ns. The analog readout speed for 30 fps is 2.5 MHz. Subtraction of the sampled values from each other is done off-chip. Additional circuitry to remove offsets deriving from the column amplifiers has been implemented. The chip is controlled by an FPGA which sends the number of the row to be accessed next and which cycle (HDR or DS) has to be applied. The execution of the cycle itself is controlled on chip. The algorithm for the calculation of the row sequence consists of a small lookup table (40 byte) and needs to execute two additions to calculate the next row number. An integration of this algorithm on a later version of the vision chip would be easy, especially because it can be used to control imagers of arbitrary resolution by only doubling the size of the lookup table.

EXPERIMENTAL RESULTS

In Fig. 4 the measured response curve of the sensor is shown. The light source used here was a spectrally flat Xe arc lamp. A bandpass filter (400 nm-730 nm) restricted the measurement to the visible part of the spectrum to allow a fair comparison with other sensors. Neutral density filters were used to vary the incident light intensity. The signal of the sensor is denoted in arbitrary units, it is the mean signal of the HDR window. Integration time regulation was programmed here to regulate from $T_{max} = 33$ ms to $T_{min} = 4\,\mu$s resulting in a frame rate of 30 fps. As could be seen the sensor is able to cover intensities in the region from $0.9\,\text{mW/m}^2$ to $5\,\text{kW/m}^2$ under these conditions, resulting in a dynamic range of 135 dB.
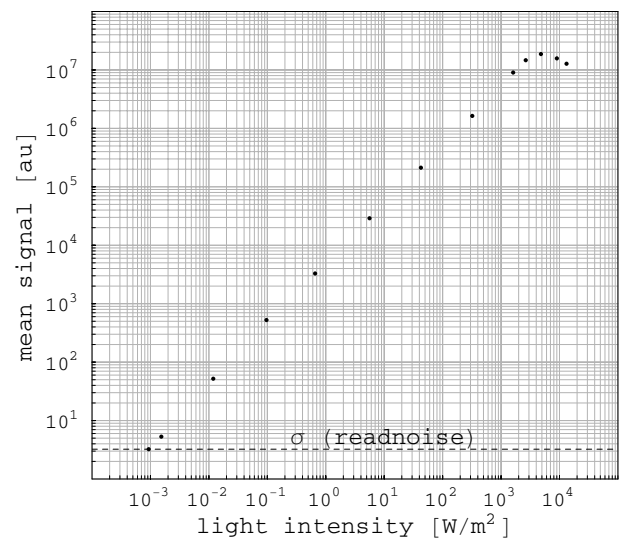
Figure 4. *Averaged photoreceptor response with activated integration time regulation.*

At high intensities a decline of the sensor's signal is observable. The reason for this is the reduction of the reset
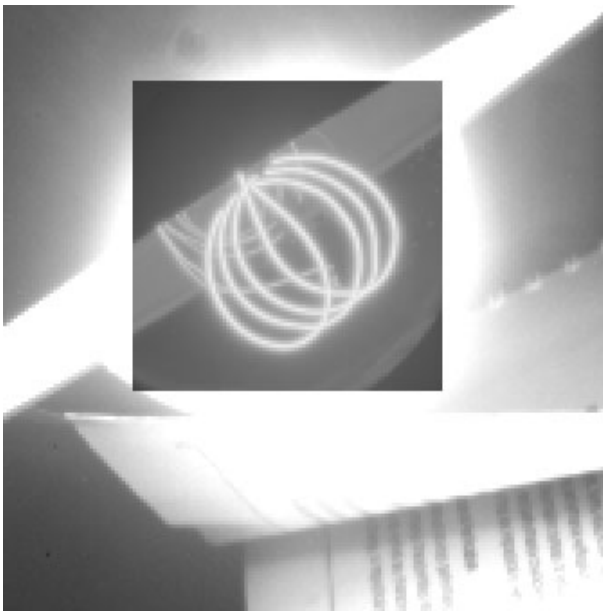
Figure 5. *Sample image taken with activated HDR window.*

values by the incident light before this value is sampled on the corresponding capacitor. Even though this effect could be further reduced by a specific reduction of sampling durations for reset values of very short integration times, it is not completely avoidable. On the other side inspection of the reset values always indicates reset reduction and thus permits to discriminate deteriorated values.

Figures 5 shows a sample scene taken with the presented CMOS image sensor. The recorded scene consists of a bright incandescent lamp (carbon filament) illuminating a writing, not yet tapping the full potential of the sensor (scene exhibits a dynamic range of 80 dB in intensity). Fixed pattern noise deriving from the device-to-device mismatch of pixel and column amplifiers circuits has been corrected by the integrated double sampling. The scene has been recorded with activated HDR window. Here, the signal voltage after integration is combined with the individual integration time for each pixel to get the final HDR image. Table 1 summarizes the technical data of the chip.

Table 1. Technical data of the image sensor.

Technology	0.25 μm CMOS
Resolution	170 x 170
HDR window	85 x 85
Pixel pitch	7.5 μm
Photodetector	n^+-diff. diode
Fill factor	40 %
Power consumption	2.5 mW
SNR (at 270 mW/m^2)	48 dB
Dynamic range	135 dB

SUMMARY

A scheme for adaptive integration time control based on on-chip multiple sampling has been presented. It has been implemented in a prototype CMOS HDR imager offering a resolution of 170 x 170 pixels. Flexibility is a key element of the implementation: The chip features a foveal HDR region (sliding window) which can be moved under external control across the sensor surface. The size of this region is here 85 x 85, it depends on the size of the SRAM which the designer is willing to implement on chip. Averaging of neighboring pixels has been successfully tested. It can be combined with HDR expansion which therefore enables the chip to get HDR over the whole sensor array in a single shot. Maximum and minimum integration time can be chosen as well as gradation of the integration time regulation to adapt the sensor to different applications. Further advantages are easy image reconstruction and small pixel sizes by the use of a slightly modified standard APS. The resulting images are free of visible artifacts. A dynamic range of 135 dB at 30 fps has been reached making the chip a unique tool for scene inspection under difficult illumination conditions.

REFERENCES

[1] M. LOOSE, K. MEIER AND J. SCHEMMEL *A Self-Calibrating Single-Chip CMOS Camera with Logarithmic Response.* IEEE JSSC, vol.36, 1146-1152, 2001.

[2] S. DECKER, R. MCGRATH, K. BREHMER AND C. SODINI, *A 256x256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output.* IEEE JSSC, vol.33, no.12, 2081-2091, 1998.

[3] O. YADID-PECHT *Wide-dynamic-range sensors.* Optical Engineering, vol.38, no.10, Oct. 1999.

[4] O. YADID-PECHT, A. BELENKY *In-Pixel Autoexposure CMOS APS.* IEEE JSSC, vol.38, no.8, 1425-1428, Aug. 2003.

[5] B. J. HOSTICKA ET AL. *A 1K 1K High Dynamic Range CMOS Image Sensor With On-Chip Programmable Region-of-Interest Readout.* IEEE JSSC, vol.37, no.87, 911-915, 2002.

[6] A. SIMONI ET AL. *Novel CMOS Image Sensor With a 132-dB Dynamic Range.* IEEE JSSC, vol.37, no.12, 1846-1852, 2002.

[7] D. YANG AND A. EL GAMAL *Comparative Analysis of SNR for Image Sensors with Enhanced Dynamic Range.* Proc. SPIE, vol.3649, 197-211, 1999.