Readout of the OTIS for the Outer Tracker

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- Readout schemes
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- Project status
  - DLL
  - Pipeline/DBuffer
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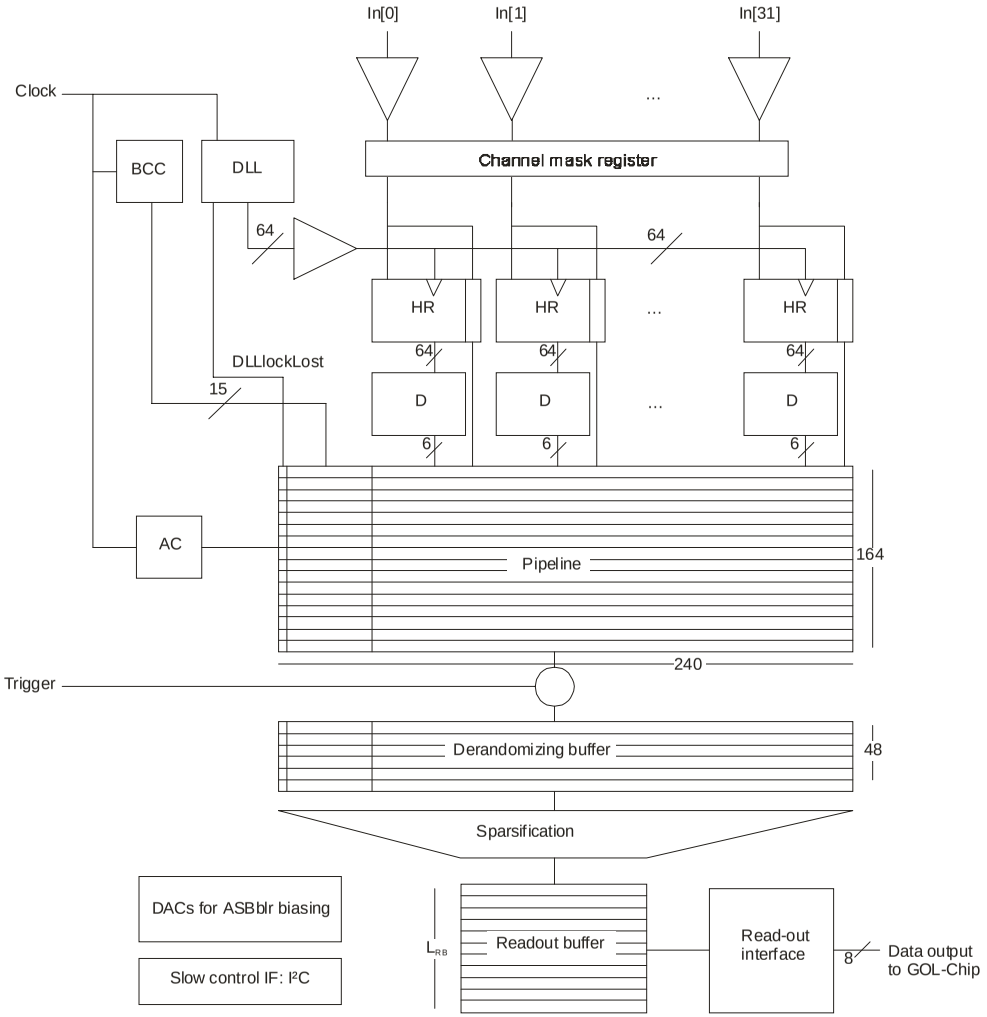
- Summary

Introduction



Data Flow:

- Pre-Pipeline
- Pipeline
- Readout (2 modes)

Requirements:

- Synchronous TDC readout
- Readout time $\leq$ 900ns

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Readout 1: plain hitmask

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- Max. readout time: 900ns
- Truncation of readout sequence after 900ns.
  (Hit information stays, only drift times lost)
- Next event not earlier than 900ns after previous one.

⇨ 900ns readout time garanteed.

⇨ All TDC stay synchronous.

Readout 1: plain hitmask

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- Data format for 1, 2 or 3 BX per trigger (programmable)

1 BX per trigger (100% mean occupancy w/o truncation)

Bit	0..31	32..63	64..69	...	58+(6n)..63+(6n)
Data	Header	1 Hitmask	Drift time1	...	Drift time n

2BX per trigger (50% mean occupancy w/o truncation)

Bit	0..31	32..95	96..101	...	90+(6n)...95+(6n)
Data	Header	2 Hitmasks	Drift time1	...	Drift time n

3 BX per trigger (27% mean occupancy w/o truncation)

Bit	0..31	32..127	128..133	...	122+(6n)...127+(6n)
Data	Header	3 Hitmasks	Drift time1	...	Drift time n

Readout 2: encoded hitmask

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- Single hit TDC:
  Only first hit out of 1, 2 or 3 BX transmitted.
- Independant from occupancy.

⇨ 900ns readout time garanteed.

⇨ All TDC stay synchronous.

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Dirk Wiedner Heidelberg University

Readout 2: encoded hitmask

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- Data format: first hit out of 1, 2 or 3 BX (programmable)

  (independant from occupancy)

Bit	0 .. 31	32 .. 39	...	280 .. 287
Data	Header	Drift time 0	...	Drift time 31

- 8 bit drift times (2bit hit position, 6bit drift time)

Hit Position	Data
1. BX	00xxxxxx
2. BX	01xxxxxx
3. BX	10xxxxxx
No Hit	11xxxxxx

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Status - DLL

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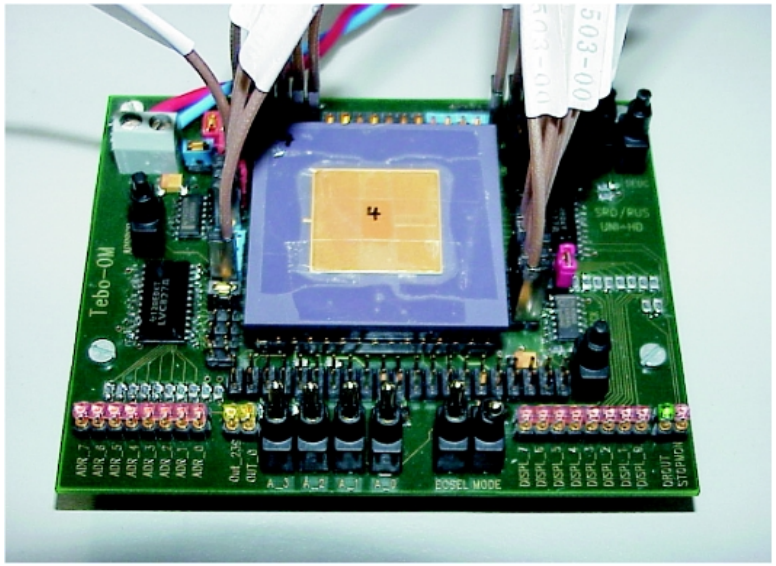
- Differential non linearity (DNL)

Rio:

DNL = 0.79 bin

(with 1.6ns pulse width,

and approx. $1.6 \cdot 10^5$ hits)



Problem with setup not understood

Actual:

DNL = 0.47 ± 0.03 bin w/o Memory

DNL = 0.51 ± 0.03 bin with Memory

(with 1.6ns pulse width,

and approx. $2.4 \cdot 10^6$ hits)

Status - Pipeline/DBuffer

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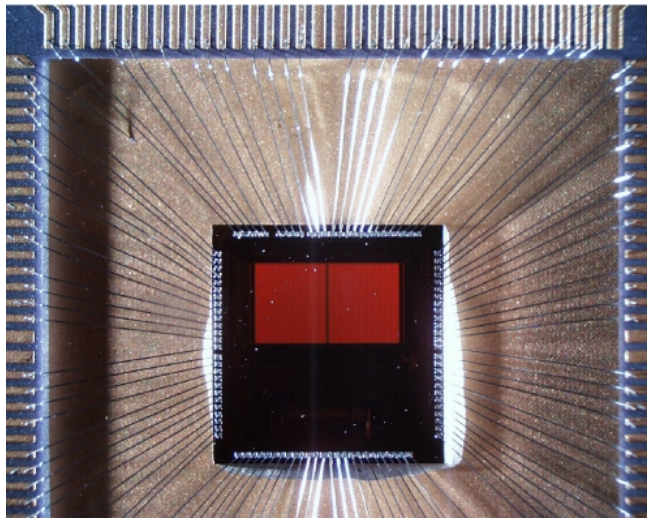
- SRAM Testchip:

  Measurements prove expected timing constraints.



- Teststructure Derandomizing Buffer:

  First functional test successfull.

  Exact timing constraints yet to be measured.

Status - Control Algorithm

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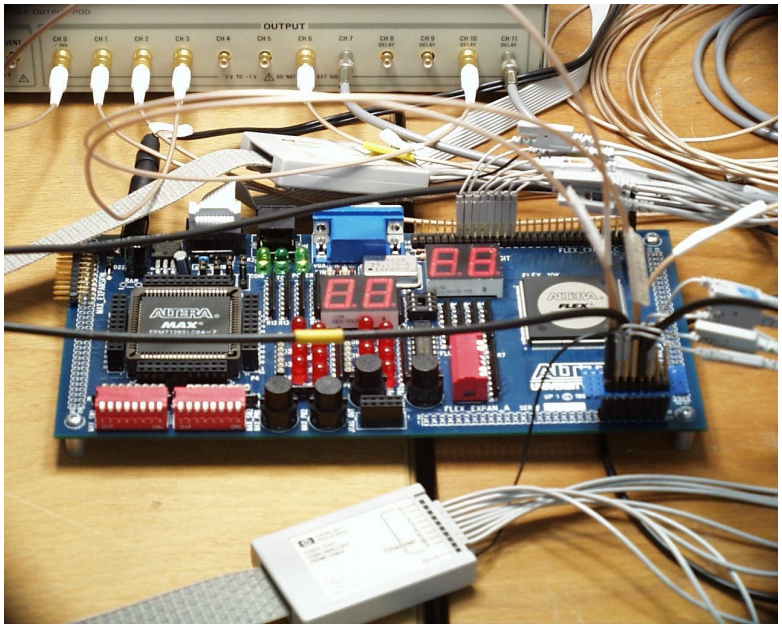
- Pipeline/DBuffer Control Algorithm:

  Simulated, synthesised for ASIC/FPGA. Errors found with FPGA test are corrected.



- Readout Control Algorithm:

  New implementation under work. FPGA test planned.

Status - I²C Interface, DACs

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- I²C interface and DACs can be taken from the Beetle chip.
- I²C interface fully functional, SEU robust version currently under test.
- Only minor changes needed for the DACs.

Summary

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- Readout schemes fulfill LHCb requirements.
- Parts ready for prototype assembly:
  - Pipeline
  - I^2C Interface, DACs
- Further effort needed for:
  - Understanding the DNL-Measurement
  - Characterisation of DBuffer
  - Coding and testing of readout algorithm