The Pipeline Control logic

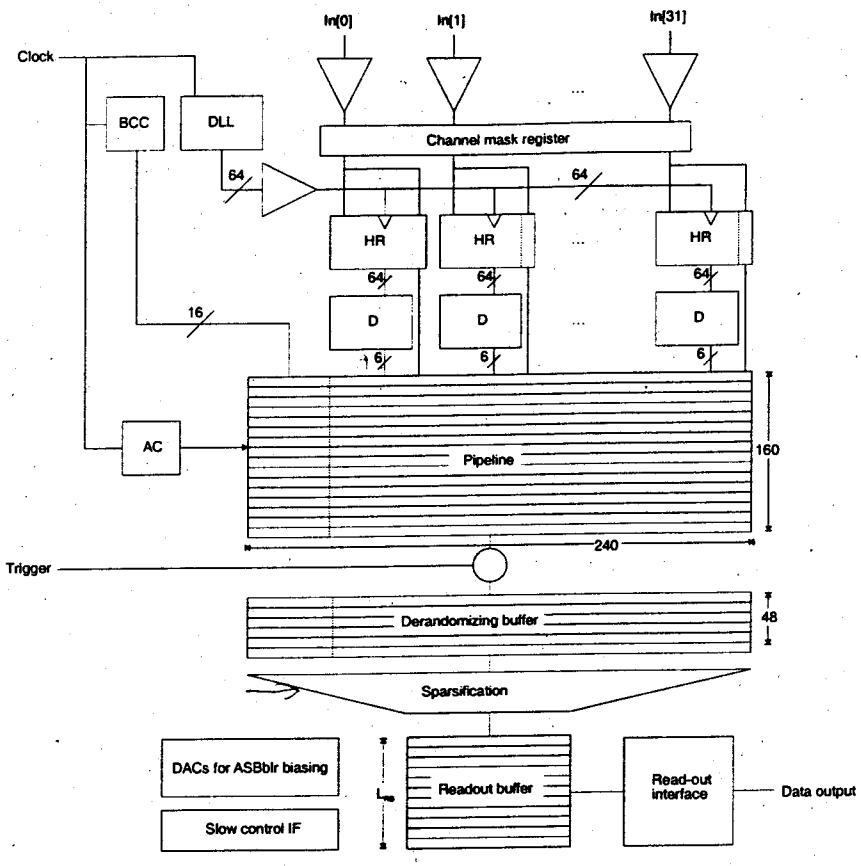


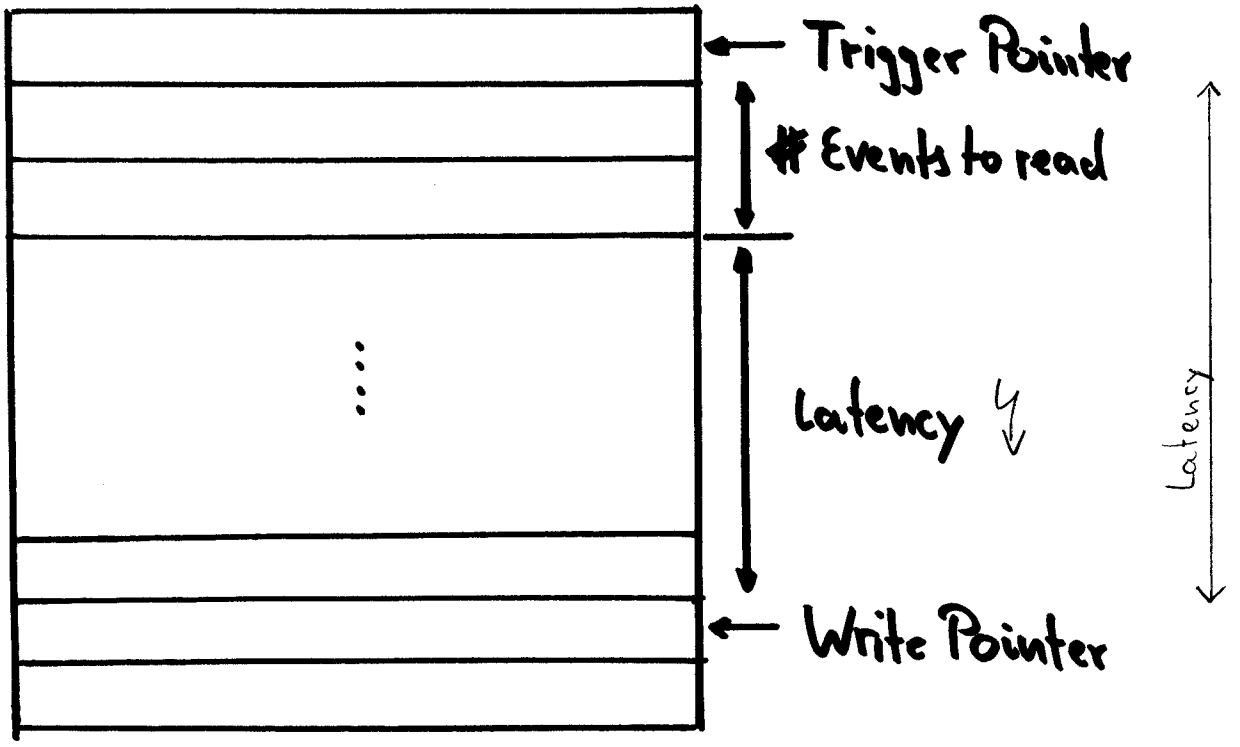
Figure from LHCb Note 2000-15

Different Readout Modes

consecutive mode : drifttimes of up to three consecutive bunchcrossing intervals are read out (w/o sparsification) per trigger

Hit Scanner Mode : only the first hit inside a sequence of up to three bunchcrossing intervals is readout per trigger/channel (w/o sparsification)

The control logic behaves equal for each mode. It has to copy up to three data words per trigger from the pipeline to the derandomizing buffer.

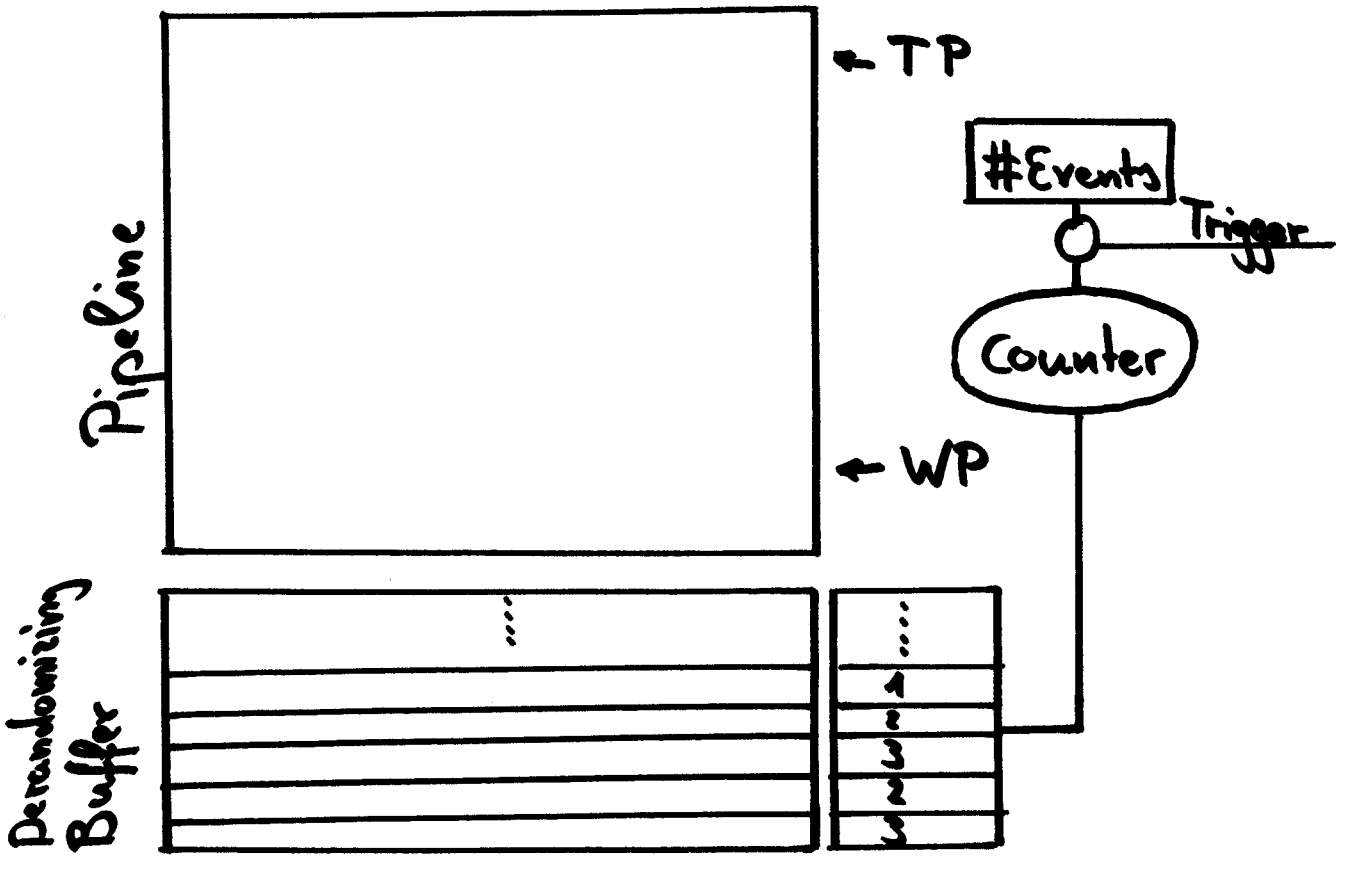


Write Pointer: points to the location where new data is written to the pipeline (synchronous to LHC clock)

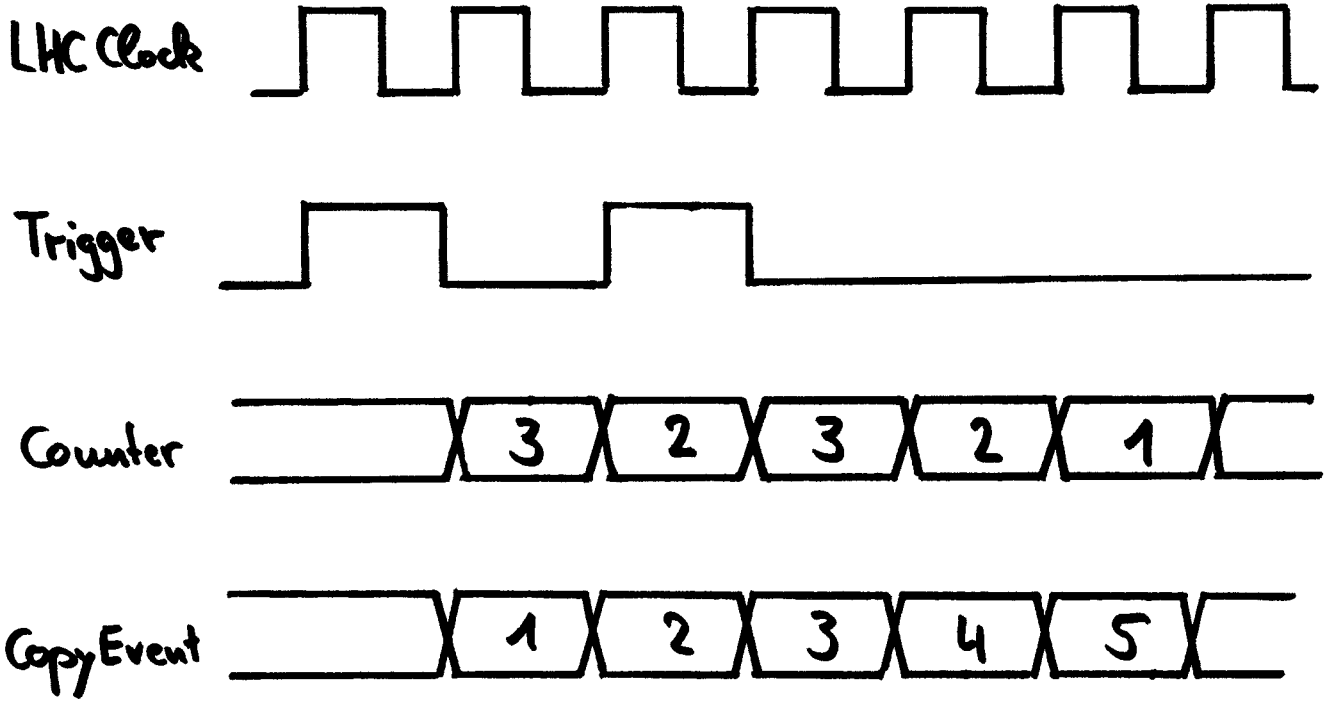
Trigger Pointer: points to the pipeline location from where data is read per trigger

The distance between WP and TP is the composition of latency and the number of events to read out per trigger.

To take count for consecutive trigger the number of events to read out is added to each data word.



If there is a trigger for example at Bx n and n+2 and the number of events to readout is three, then 5 data words are copied to the derandomizing buffer with 3;2;3;2;1 added.


LHC Clock
Trigger
Counter
3
2
3
2
1
CopyEvent
1
2
3
4
5

Testenvironment

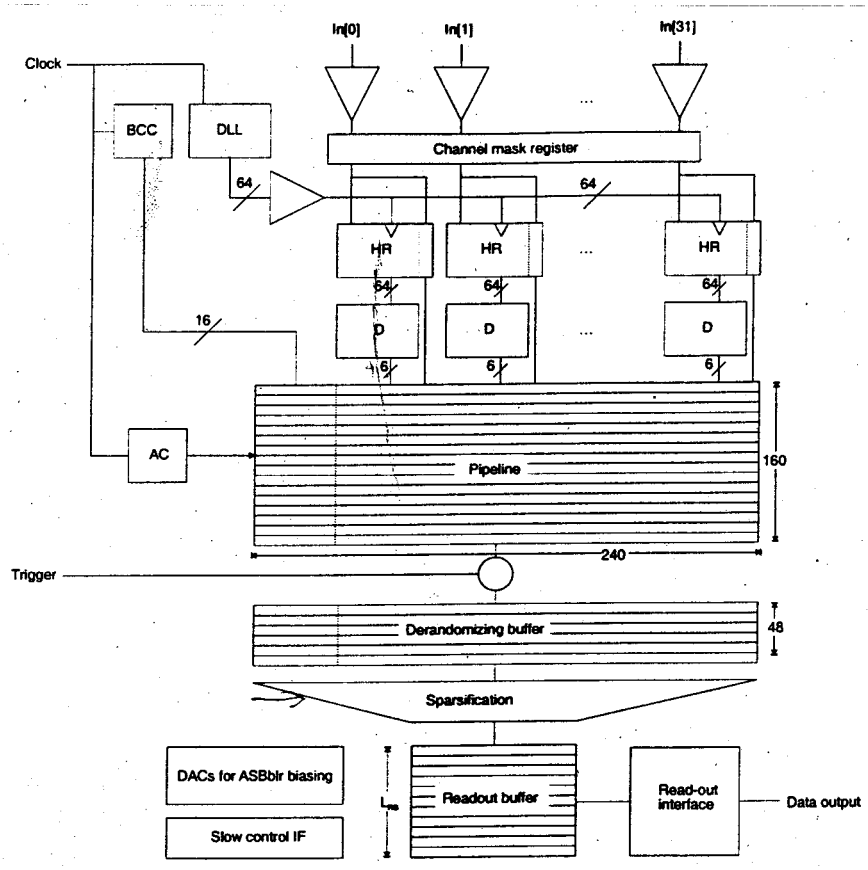


Figure from LHCbNote2000-15

- Verilog model of the SRAM to take count for setup and hold times
- "off line" calculation of random hits and drift times with parameterised
  - ASDBlr dead time (20ns)
  - number of channels (32)
  - maximum drift time (50ns)
  - occupancy (10%)
- Hits for neighbored channels are not(yet) correlated
- Simulation data gets inserted direct to the pipeline (clock synchonous)

Next Steps

- Finish programming and simulation of the pipeline control logic.
- Synthesis, implementation and test of control logic on a FPGA.
- Start programming of sparsification and readout logic.