A Hartmann-Shack Wavefront Detector realized with an ASIC

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Abstract

A smart sensor CMOS-ASIC has been developed for the application in a Hartmann-Shack optical wavefront sensor as image detecting and processing module. The ASIC includes a matrix of photosensitive devices and mixed-signal processing circuitry, evaluating photo currents for characteristic properties. The main task of the ASIC's signal processing unit is to process the characteristic focal point matrix of the Hartmann-Shack sensor's optical lens array exposed to the measured wavefront. Detecting the lateral deviation of each focal point caused by the partial distortion of the wavefront within the according lens, the phase information of the light beam can be retrieved. In intention of measuring optical distortions of the human eye only a very low optical incident power is allowed. Thus, reducing the amount of generated photo currents to some ten pA, most of the analog signal processing MOS-FET devices conduct subthreshold currents. To realize an oversampling of the eyes' inherent movements, the system's frame repetition rate of measuring the wavefronts distortion is chosen to be as fast as 1 kHz. The ASIC is realized in a standard industrial 0.6 μm n-well CMOS process with single poly and triple metal. Its dimensions are $7.7 \times 8.2\, mm^2$.

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I. Introduction

One single path measurement commonly applied in an optical wavefront detection system is referred to as the Hartmann-Shack wavefront detection scheme. A Hartmann-Shack-Sensor (HSS) consists of an array of optical lenses placed within the optical path to divide the incident light beam into a matrix of subapertures, ref. to Fig. 1 a). Each lens focuses into a focal point located within the lens array's focal plane. In case of a local tilt of the wavefront within the margins of the lens, the focal point is deviated perpendicular to the optical axis, ref. to Fig. 1 b). The amount of deviation is proportional (in first order) to the amount of the local tilt of the wavefront and therefore allows the tilt's quantification. The reconstruction of the light beam's total wavefront is feasible by means of a least-square-fit of the measurement data of all focal point deviations. The mathematical description of the optical path difference (OPD) between the calculated wavefront and an arbitrary reference wavefront thereby is commonly based on high order two-dimensional *Zernike* polynomials [1], [2].

Today's systems are capturing the focal points by means of CCD arrays. The signal processing of the focal point deviation is executed with digital signal processing architecture enabling a high resolution in OPD reconstruction, at the expense of repetition rate and thus real time performance. In this paper an ASIC is presented, combining photo sensitive devices for image detection and electrical circuits for focal point position determination. Analog circuitry is used to evaluate focal point intensity distributions by use of MOS-FET device characteristics with inherent parallelism, offering a repetition rate which is only limited by the absolute height of generated photo currents and reaches easily rates of several hundred Hz, thereby reducing the resolution of OPD reconstruction compared to digital systems.

With the intention of measuring the optical performance of human eyes in a double-path measuring method as presented in [3] and [4], a trade-off between repetition rate and

resolution has to be considered. Taking care of security efforts when directly penetrating the eye's retina by measuring beams, the reflected light beam's incident power reduces to levels below 0.01 W/m^2. The amount of photo current generated by the photo sensitive devices of the ASIC thus reduces to some ten pA and the analog signal processing circuitry needs to cope the large transient delays of MOS-FET devices conducting subthreshold currents.

II. The System

The Hartmann-Shack wavefront detector consists of a lens array mounted in parallel to the photo detector matrix in distance of the focal length of the lens array. The light beam is passing the lenses and in case the partial wavefront within the margins of a lens is tilted, the focal point is deflected, ref. to Fig. 2 a).

According to the rules of paraxial optics ($sin\ x = x$), this deflection Δx is calculated applying

$$\frac{dW}{dx} = \frac{\Delta x}{f}, \tag{1}$$

with dW/dx as the tilt of the wavefront in X-direction and f as the focal length of the lens array. To derive some practical values, a wavefront tilt of about $dW/dx = 200\ nm/400\ \mu m$ results in a focal point deviation of $\Delta x = 26.5\ \mu m$, basing $f = 53\ mm$.

The lateral intensity distribution of a focal point equals a Gauss-distribution, ref. to Fig. 2 b). More exact Fourrier-Optics models an intensity distribution with a peak value in the center and concentric circles of decreasing intensity with minima and maxima of higher order. The diameter D_F of the first minimum-intensity circle is often referred to as the diameter of the *Airy-Disc*. It's value is

$$D_F = 1.22 \cdot \lambda \cdot f / D_L \tag{2}$$

and with $\lambda = 780\ nm$ as the light beam's optical wavelength and $D_L = 400\ \mu m$ as the lens diameter, $D_F = 126\ \mu m$. Thus, the focal point's deviation Δx of 26.5 μm is small

compared to its width D_F of 126 μm and the signal processing circuitry needs to evaluate the location of the maximum intensity by clearly distinguishing only slightly differing values.

In Fig. 3 the arrangement of the two elements of the HSS, i.e. the lens array and the ASIC with its various signal processing modules is shown. For easy readability, only 4×4 lenses and clusters for focal point position detection are drawn, whereas the ASIC includes 16×16 clusters for the position detection of 256 focal points. Each cluster contains an array of photo diodes and surrounding analog signal processing circuitry to locate the focal point's intensity maximum. After detection, the generated data is transferred to digital circuitry, where reformatting and compression of position data takes place and finally, the data is sent to the outside of the ASIC for least-square-fit calculation of the Zernike polynomial coefficients.

Each cluster is divided into an array of vertically and horizontally connected photo detector stripes and surrounding signal processing for position detection, as shown in Fig. 4 b). The photo currents which are generated by these stripes are evaluated in parallel in the circuit blocks *current detector*. Following the function of a Winner Take All (WTA) topology, the peak currents of the X and Y directions are located and the position is digitized to binary values. All clusters are linked together by the modules *data shift*, which are loaded with the according position values after an integration period. Applying a daisy-chain configuration, these modules are used to shift the X- and Y-position of all 256 focal points to the digital module for compression, ref. Fig. 5.

The lateral dimensions of one cluster of 400×400 μm^2 fit to the lens diameter. To allow a maximum area for focal point position detection, thus enlarging the dynamic range for wavefront measurement, an area restriction to the analog signal processing circuitry is given. At the same time, the granulation of photo detector stripes needs to be high enough to enable an adequate resolution of position detection and thus the complexity of signal

processing circuitry enlarges. This tradeoff between resolution and dynamic range needed to be carefully considered. The chip area of the signal processing circuitry has been kept as small as possible to enlarge the photo sensitive area and thus to allow a proper dynamic range of the focal point position detection.

In the following two sections, the various signal processing modules are presented in detail.

III. The Photodetector Matrix

In the proposed wavefront detection ASIC, the p+/n-well-diode is used as photo sensitive device. Although its quantum efficiency is less than that of the n+/p-substrate-diodes, which occupy the same die area, the p+/n-well-diodes are applied. The reason is based on circuit connectivity demands and will be presented in detail in section IV-B.

Within the photo detector array of one cluster, the photo diodes are placed in a special pattern. The array contains a number of 19×19 photo detector pixels, each consisting of two adjacent photo diodes covering an area of $p^2 = 17.6 \times 17.6\ \mu m^2$. The left diode is connected to its column neighbors and the right diode is connected to its row neighbors, ref. to Fig. 4 a). Thus, a number of 19 stripes in each direction is realized, allowing to readout the stripe currents of X- and Y-direction simultaneously. Effects off asymmetry due to this arrangement can be neglected because of the large focal point diameter compared to the small outline of a single photo diode. Fig. 6 shows a cut through the wafer along a vertical stripe (mark A in Fig. 4), showing the intensity distribution of a focal point. Each horizontal photo diode stripe is illuminated by fractions of the incident power within the length p and the row currents I_n are generated.

Applying the equation of photo current generation by charge carrier generation due to absorption of photons

$$I_{ph} = \frac{q\,\eta\,P\,\lambda}{h\,c} \tag{3}$$

with q as the elementary charge, η as the photo diode quantum efficiency, P as the optical

power, λ as the photon wavelength, h as the Boltzman constant and c as the light velocity in vacuum, the amount of generated photo current per stripe can be calculated by integrating the focal point intensity distribution partially within the margins p of the single stripes. To estimate the quotient of $I_n/I_{n\pm1}$, measured data of a focal point intensity distribution is considered. Due to non ideal properties of the lens, the focal point diameter is enlarged to $D_{FM} = 200\ \mu m$ compared to the ideal 126 μm and the quotient of $I_n/I_{n\pm1}$ is about 1.08, according to a difference of only 8% in photo current generation between the centre stripe and its neighbors. The absolute value of the center current, which is generated due to a focal point incident power of $P = 10\ nW\ @\ \lambda = 780\ nm$, is $I_n \approx 50\ pA\ @\ \eta \approx 0.1$.

The difference in currents of about 8% is only valid if the centre of the spot is located directly above the photo diode stripe. Naturally, the peak intensity will be randomly located, and it might happen that two neighbored stripes are illuminated with the same amount of incident power. In this case, the detection result will be statistical and the decision, which current is the highest, is based on noise and mismatching properties of the signal processing circuitry. Section IV-C will consider these problems in detail.

IV. The Circuitry

The most important part of the ASIC's signal processing circuitry is the current detector for locating the maximum current among the 19 generated photo currents. As mentioned before, the WTA topology is used, detecting the maximum of several input currents by use of device characteristics of MOS-FETs.

A. Application of a WTA algorithm

Fig. 7 shows the basic circuit of the WTA topology as presented in [5], which since then has been further examined in various research projects [6]-[12]. Three cells are drawn for the detection of three currents. Each cell consists of the two MOS-FETs M_S and M_F.

M_S senses the input current I_i and generates a V_{DS}, which is linked to the gate potential of M_F, ref. to Fig. 8. For the reason that all M_S are gate-connected, owing the same I_D vs.

V_{DS} characteristics, one of them will generate the highest drain potential due to its highest I_D (I_i) and the V_{GS} of the according M_F will also be the highest of all M_F. Therefore, most of the current of the current source I_{SRC} will be sunk by this M_F and guided to I_o, inhibiting current flow of the other M_F.

To estimate the operating point of two WTA-cells in weak inversion, the subthreshold drain current characteristic proposed in [13], extended by a channel length modulation factor, is used:

$$I_D = S\, I_{D0}\, e^{\frac{V_{GB}}{n\, V_t}} (e^{-\frac{V_{SB}}{V_t}} - e^{-\frac{V_{DB}}{V_t}})(1 + \lambda(V_D - V_S)). \tag{4}$$

I_{D0} and n are representing process characteristics, S the effective width over length ratio of the channel, λ the channel modulation factor and V_t the temperature voltage kT/q.

Using the input photo currents of $I_{Ph1} = 50\ pA$ and $I_{ph2} = 46\ pA$, a source current of $I_{SRC} = 60\ nA$ and typical process parameters, the solution sketched in Fig. 9 is achieved. The small difference in input currents creates a large difference in the V_{DS} of M_{S1} and M_{S2}, which are used to control the gates of M_{F1} and M_{F2}, respectively. M_{F1} will source most of I_{SRC} as M_{F2} is shut off being controlled by a negative V_{GS}.

The transient response of a cell is mainly based on the amount of capacitance at the drain nodes of M_{Sn}, $C_{\Psi 1}$ and $C_{\Psi 2}$, ref. Fig. 8. In case the input currents are changing from the state $I_{ph2} < I_{ph1}$ to $I_{ph2} > I_{ph1}$ at a constant I_{ph1}, three time steps occur until the output current changes significantly. In step one, the photo current I_{ph2} changes to a higher amount, but the gate potential of M_{S2} keeps stable, as it is still defined by M_{S1} and M_{F1}, and the parasitic capacitor $C_{\Psi 2}$ is charged by $\Delta I2 = I_{ph2} - I_{D2}$ to raise V_{DS} of M_{S2}. In step two, V_{DS2} is high enough to significantly affect the current through M_{F2}. Now, M_{F2} inhibits the current flow through M_{F1} by increasing its drain current to almost I_{SRC}, and the gate potential of M_{S1} and M_{S2} changes to a slightly higher value. In step three, the capacitor $C_{\Psi 1}$ is discharged, reducing the drain potential of M_{S1} to its equilibrium value. The last time step is not important for the response time, because

output currents are already changing in the second section slightly behind the cross over of the drain potentials of M_{S1} and M_{S2}. The first step of recharging the parasitic capacitor $C_{\Psi 2}$ dominates the response time by far, because of the small amount of ΔI for charging and the large capacitance of $C_{\Psi 2}$ to be charged.

Fig. 10 represents a simulated transient response, where V_{DS} and V_{GS} of M_{S1} and M_{S2} are shown, together with the output currents I_{o1} and I_{o2}. To estimate the response time, all parasitic capacitors of the drain node at M_{S2} are taken into account: the junction capacitors of the photo diodes of one stripe, the junction capacitor of M_{S2}'s drain and the gate capacitor of M_{F2}. The junction capacitor of the photo diode stripe is derived from the area of each of the 19 diodes and some process parameters and evaluates to $C_j \approx 2.3\ pF$ at a reverse voltage of $V_j = -2\ V$. This value exceeds the other two contributions of the terminal capacitors by orders of magnitude. Assuming a change of the photo current from $I_{ph2} = 46\ pA$ to $I_{ph2} = 54\ pA$ at a constant $I_{ph1} = 50\ pA$, it takes $t \approx 0.6\ s$ to raise V_{DS} of M_{S2} by $1V$ from the initial value to change the output current conditions of the two cells significantly. To decrease this large value of transient response time, different extensions to the basic WTA topology have been evaluated.

B. Acceleration of the transient response

Apparently, the largest influence to the response time of the WTA-cells is given by the huge amount of capacitance of C_j. To reduce the value appearing at the drain nodes of the M_{Sn}, a regulated cascode configuration as shown in Fig. 11 was introduced. It can be shown, that a suppression of the junction capacitor by a factor of $(\lambda\, n\, V_t)^2$ is achieved. The resulting parasitic capacitor at the drain nodes of the M_{Sn} is then dominated by the drain junction capacitor of M_S and the gate capacitor of M_F. Based on process parameters, the time scale of Fig. 10 will reduce by a factor of $C_j/C_\Psi \approx 45$, and it takes about $13\,ms$ to change the output current conditions significantly.

Another improvement of response time can be achieved by setting the node potential

of the drain of M_{Sn} to a defined value, which bypasses the first time step. Introducing the transistors M_{In} at the nodes Ψ_n, as shown in Fig. 12, a startup value of for example $V_{init} = 0.9\ V$ can be set, which is about $200\,mV$ less then the crossover point of the V_{DSn} of Fig. 10. As all M_{Fn} are then conducting the same I_D ($\sum I_D(M_{Fn}) = I_{SRC}$), V_{GS} of the M_{Sn} is forced to a considerably low value, nearly shutting of the M_{Sn}. Releasing the nodes Ψ_n for an integration time t_{int}, the capacitors $C_{\Psi n}$ are recharged by the complete photo currents, as long as $V_{GS}(M_{Sn})$ still avoids significant current flow in the M_{Sn}. In case photo current I_{phi} is highest, M_{Fi} will source most of I_{SRC}, inhibiting current flow in the other M_{Fn}, and the cell wins. Due to the effect of recharging the capacitors Ψ_n with the complete photo current and not only with the difference of photo currents, an acceleration in response time by a factor of about one order of magnitude is achieved by carefully choosing V_{init}.

For further response acceleration, a positive feedback has been introduced into the WTA topology, as suggested in [7], which feeds an amount of the output current back to the input current of each cell, therefore boosting the effect of charging the capacitors $C_{\Psi n}$. To adapt large output currents to the small input photo currents, a positive feedback with a controllable amount of feedback gain (attenuation) has been evaluated in this project as a new feedback topology. Therefore, a PMOS-FET current mirror is added, where the mirror gain is controlled via the body-effect[1] of the output MOS-FET, ref. to Fig. 13. The amount of current, which is fed back to the input node, is evaluated by considering eq. 4 for the body-effect, resulting from applying different potentials to the source and bulk terminals of M_{FB}. The fraction of I_{out} to the feedback current I_{fb} is given by

$$\frac{I_{out}}{I_{fb}} = e^{V_{SB}(n-1)/\,n\,V_T}. \tag{5}$$

[1] As only the body-effect of a PMOS-FET can be controlled arbitrarily in p-substrate CMOS-process, the whole WTA-circuit topology needed to be designed for p-channel feedback-mirror, which arises the need for p+/n-well diodes as photo sensitive devices, as mentioned in chapter III.

It can be shown by simulations, that if the feedback current is well adapted to the amount of input current, a further increase in speed can be achieved.

Applying all the former described topology changes to the basic WTA-configuration, a reduction of transient response time to less than 1 ms has been achieved using same conditions as compared to the 0.6 s of Fig. 10. Of course noise and mismatching properties also increase, thus the influence of parasitic effects will be discussed in the following section IV-C, and in chapter V practical results of these effects will be summarized.

C. Noise and mismatching considerations

When talking about currents in the range of pA, the question for noise and mismatching properties arises. To estimate the behaviour of the WTA-cells, a consideration of the sensitive gate potential of M_{Fn} is made by applying two voltage sources to the gate. The first one is used to model the noise voltage $\overline{v_n^2}$, the second one to model the effect of mismatching with an offset voltage v_{os}, ref. to Fig. 14.

To derive $\overline{v_n^2}$, different noise sources are considered. First, applying Poisson's distribution of uncertainty in counting single events, the number of noise electrons being accumulated by the capacitors C_{Psi} can be calculated with the total capacitor's charge Q by

$$n_n = \sqrt{N} = \sqrt{\frac{1}{e}\,Q}. \tag{6}$$

The first contribution of noise to $\overline{v_n^2}$ results from the photo diodes' photo current and leakage current and from the amount of feedback current and can be derived from

$$\overline{v_{n1}^2} = (e\,n_n\,\frac{1}{C_\Psi})^2 = e\,\frac{Q}{C_\Psi^2} = e\,\frac{1}{C_\Psi^2}\int_0^t I_{ph} + I_s + I_{fb}\;d\tau. \tag{7}$$

Another contribution is given from Reset-noise by setting the capacitor C_Ψ to a defined value before the integration period. During this phase, the capacitor is charged to a voltage with an uncertainty resulting from thermal noise of resistors. The amount of noise can be calculated by considering the spectral density of current noise and impedance at the node

Ψ:

$$\overline{v_{n2}^2} = \int_0^\infty \frac{2\,e\,(I_{ph} + I_s + I_{fb})}{\left|j2\pi f C_\Psi + g_{ds(MI)} + g_{ds(MS)}\right|^2}\,df. \tag{8}$$

Next, when M_I is shut off, some electrons are pushed to the node Ψ due to charge feed through from the gate of M_I. The number of electrons is

$$n_i = \frac{1}{e}\,C_\Psi\,\Delta V. \tag{9}$$

Using again Poisson's distribution, this will give the third contribution of noise to $\overline{v_n^2}$ with

$$\overline{v_{n3}^2} = \frac{1}{C_\Psi^2}\,(\sqrt{n_i}\,e)^2 = \frac{1}{C_\Psi}\,e\,\Delta V. \tag{10}$$

The fourth and fifth contribution to $\overline{v_n^2}$ results from the flicker and thermal noise of the channel current of M_F being transformed to the gate of M_F with

$$\overline{v_{n4}^2} = \int_0^{f_0} \frac{KF}{2\,f\,C_{ox}\,WL\,K'}\,df \tag{11}$$

$$\overline{v_{n5}^2} = \int_0^{f_0} \frac{8\,k\,T}{3\,g_m}\,df. \tag{12}$$

The bandwidth of the transfer-function of M_F can be calculated with small signal analysis of I_{SRC}, M_F, M_M and the parasitic capacitors C_κ of the node κ to

$$f_0 = 1.57 \cdot f_1 = 1.57 \cdot \frac{1}{2\,\pi}\,\frac{g_{m(MM)} + g_{ds(MF)}}{C_\kappa}. \tag{13}$$

The relation $f_0 = 1.57\,f_1$ takes a transfer function with a single pole at $f = f_1$ into account.

Due to the independence of all considered noise contributions $\overline{v_{ni}^2}$ the sum of each source will give the amount of equivalent noise $\overline{v_n^2}$ of Fig. 14:

$$\overline{v_n^2} = \sum_{i=1}^{5} \overline{v_{ni}^2} = \overline{v_{np}^2}(I_{ph}) + \overline{v_{nc}^2}, \tag{14}$$

$\overline{v_{np}^2}(I_{ph})$ models the noise which depends on the amount of charge of the capacitor C_Ψ accumulated by the photo current I_{ph}, and $\overline{v_{nc}^2}$ models the current independent noise.

Assuming a photo current of $I_{ph} = 10\,pA$ is accumulated on C_{ψ} during an integration period of $t_{int} = 1\ ms$, and deriving (14) numerically with typical process parameters, the fraction of uncertainty of C_{Ψ}'s voltage at the end of the integration period evaluates to

$$\frac{\sqrt{\overline{v_n^2}}}{\Delta V_{\Psi}} = \frac{2.7\,mV_{rms}}{200\,mV} \approx 1.3\%. \tag{15}$$

In case I_{fb} conducts significant current, the noise properties of the circuit depends dramatically on the ratio of I_{ph}/I_{fb}, which itself is a strong nonlinear function of $\overline{v_n^2}$ and a simple close mathematical expression could not be derived. Chapter V will summarize measurements of noise characteristics in feedback mode.

The mismatching properties of the neighboring WTA-cells are also critical for WTA-functionality. The accuracy of distinguishing input currents for differences is based on comparing node potentials from several, equally built circuit nodes. To estimate consequences of FPN the voltage source v_{os} has been added to the WTA-cell, ref. to Fig. 14. Neglecting the mismatching properties of the photo diodes stripes, most of the mismatching effects result from V_{GS} deviations of M_S, M_F and M_{FB}, from different charge injection values of M_I and from differing values of C_{Ψ}.

Summing together noise and mismatching contributions to the uncertainty in V_{GS} of M_F, there will be an amount of

$$\sigma(V_{GS(MF)}) = \sqrt{\overline{v_n^2} + v_{os}^2}. \tag{16}$$

Building the ratio of this uncertainty to the capacitor voltage difference ΔV_{Ψ} due to accumulated photo current during integration period, one can estimate the accuracy of the WTA function. Recalling the calculation of chapter III, the difference of photo currents of two neighboring stripes is at most 8% and a strong uncertainty in the decision of the WTA-circuit occurs between two directly neighbored WTA-cells, when $\sigma(V_{GS})/\Delta V_{\Psi} > 8\%$. This effect will be shown in chapter V.

V. Measurements

Fig. 15 shows a photography of the ASIC within the cavity of a 84-pin PLCC chip carrier. To enlarge the photo sensitive area for focal point position detection within each cluster of $400 \times 400\ \mu m^2$, the analog signal processing circuitry combining the WTA-cells and shifting registers has been compacted as far as possible. The position detection of one focal point is feasible within an area of $334.4 \times 334.4\ \mu m^2$, which is 70% of the cluster area. To prevent illumination of the sensible surrounding analog circuitry, the ASIC is shielded completely with a metal layer, except for the photo sensitive areas, refer to Fig. 15 c).

A. FPN measurements

To measure the mismatching properties of the WTA-cells in focal point position detection, the ASIC was mounted on a precision X/Y-table and illuminated with a single spot at variable diameter and controllable incident power of monochromatic light with a wavelength of $\lambda \approx 680\ nm$. A focal point was moved at a constant velocity of $v = 100\ \mu m/s$ across the clusters and the response of the WTA-cells was logged. The frame repetition rate was set to $f = 250\ Hz$. Thus, considering the pixel pitch of $p = 17.6\ \mu m$, the expected number of winning events of each WTA-cell in one cluster was $E = f \cdot p/v = 44$.

Results figured in Figs. 16 - 19 are taken from one exemplary cluster. In these figures, the upper diagram shows the response of the WTA-cells when moving the X/Y-table in one direction. The number of the winning WTA-cell is printed versus the single steps of movement. The lower diagram shows the number of winning events for each WTA-cell in histogram style and the standard deviation of winning events σ_w from the expected value E is derived. Due to missing left or right neighbors of the first and the last WTA-cell, the event counts of these were set to the expected value 44.

Tab. I summarizes the measurements for 4 different measuring conditions. In the first three columns, the direction of the movement, the focal point diameter D_F and the incident power P_F are listed. In the next column, the standard deviation σ_w as the mean value

of all 256 clusters is given. The last column assigns usage of response acceleration due to activated feedback.

As expected, the standard deviation of $\sigma_w = 5.9$ for X-direction and $\sigma_w = 7.0$ for Y-direction is small when using a sharp focal point diameter of $D_F = 17\ \mu m$. If positive feedback is used to allow position detection at a low incident power level, the standard deviation increases to 12.3 and 13.9 for X- and Y-direction, respectively . Enlarging the focal point diameter to $D_F \approx 180\ \mu m$ the standard deviation is measured to be 26.1 for X-direction and 29.8 for Y-direction. To explain these values by mismatching behaviour of WTA-cells, Fig. 20 shows the simulated output currents of two neighboring photo diode stripes versus the position of the movement. In case I_1 is of the same height as I_2, ideally the expected value of 44 winning events occurs for each cell. But if the photo current I_2' with $I_2'/I_1 \approx 1.05$ is compared to I_1, the number of winning events of I_2' will increase by 13. Considering both sides of this distribution, the deviation from the expected value of 44 will be 26. Thus, the ASIC suffers from mismatching properties between the WTA-cells of about 5%.

Decreasing incident power and using positive feedback, the position detection is suffering from mismatching and noise and a statement of σ_w for mismatching is not valid. Thus, the following section considers noise performance of the wavefront detection ASIC.

B. Noise measurements

Noise measurements were evaluated by use of a lens array to illuminate all 256 cluster simultaneously with static focal points. The incident power of the focal point was fixed to $P_F \approx 1\ nW$ for each point. Three different integration times of t_{int} were used to measure the focal point positions. With an integration time of $t_{int} = 1\ ms$, positive feedback needed to be activated to allow position detection, for the integration times of $t_{int} = 2$ and $4\ ms$, feedback was disabled. 1000 frames of focal point positions were captured with the ASIC and the X- and Y-data of each cluster were examined for deviations from a mean value.

Due to reasons explained in chapter IV-C, the position measurement generated slightly noisy position results within the 1000 frames. In Fig. 21 the distribution of position noise of all clusters is shown for the X- and Y-direction of an exemplary test-chip.

In feedback mode with an integration time of $t_{int} = 1\ ms$, the detection of the focal point position is suffering from an average noise level of 1.89 Px for the X-direction and 1.81 Px (Pixels) for the Y-direction. Some clusters are showing excited noise levels of 3 to 6 Px, which may result from blurred focal point intensity distributions as compared to the distributions of the other clusters. Increasing integration time to $t_{int} = 2\ ms$ and $t_{int} = 4\ ms$ and disabling feedback, the average noise level can be reduced to below 1 Px and to a maximum of at least 2 Px. Thus, enabling feedback clearly reduces accuracy of position detection. On the other hand, frame repetition rates of 1 kHz are feasible at a focal point incident power of $P_F = 1\ nW$. The accuracy of focal point position detection for integration times of $t_{int} \in \{1, 2, 4\ ms\}$ averaged from the two detection directions is 1.85, 1.30 and 0.74 Px, respectively, plus an additional error of $\pm 0.5\ Px$ for quantization. Related to the full scale dynamic range of 19 Px, this is according to relative errors of $\pm 7.5\%$, $\pm 6\%$ and $\pm 4.5\%$, respectively.

C. Measurement of optical wavefronts

To demonstrate the main issue of the ASIC to quantify wavefront aberrations, optical glasses of spectacles were measured. The optical glasses were specified in terms of spherical and cylindrical aberrations in units of Diopters (D). Thus, measurement performance of the position detection can be easily qualified comparing specifications and measuring results.

The optical glasses were fixed between laser source and lens array and the position data captured by the ASIC was fed to a least-square-fit algorithm. 100 repetitive measurements were performed with a focal point incident power of $P_F = 1\ nW$. Wavefront data was derived externally in a PC by generating the Zernike polynomial coefficients with a

least-square-fit algorithm. In table II, results formatted in terms of spherical (A_S) and cylindrical (A_C) aberrations are shown, together with their specified values. The amount of aberration is calculated as the mean value of 100 measurements, and the standard deviation from the mean value is listed as the error. The complementary signs of measured and specified values are based on the nomenclature of ophthalmologic applications.

The standard deviation from the mean value is fairly small as a result from the least-square-fit, when 16×16 coordinates are fit to a two-dimensional function of higher order. Nevertheless, the mean values suffer from relative errors of $\pm 7.5\%$, $\pm 6\%$ and $\pm 4.5\%$ of full scale, respectively, as explained in section V-B. As the dynamic range is dedicated to measure aberrations of ± 1 D, these errors relate to ± 0.15 D, ± 0.12 D and ± 0.09 D, respectively.

VI. Conclusions

The realization of an optical Hartmann-Shack wavefront detector with a standard CMOS-ASIC has been presented. As smart sensor, the ASIC evaluates the characteristic focal point matrix of a lens array for focal point position deviation due to optical aberrations of optical elements. P+/n-well photodiodes are arranged in a special pattern to generate multiple parallel photo currents, which are evaluated for peak values by aid of a WTA-circuit topology. To allow high repetition rates in position detection at very low levels of incident power of the focal points, a couple of acceleration mechanisms are implemented in the basic WTA-cell architecture. To quantify mismatching properties and noise performance of the WTA-circuitry, measurements were performed on prototype chips. At incident power levels of 1 nW per focal point and integration times of 1 ms, an error in focal point position detection of at maximum 15% of full scale range has been achieved. The error can be decreased to 9% by enlarging integration time to 4 ms. The ASIC has been tested in real time optical aberration measurement systems with repetition rates of up to 1 kHz frame repetition rate.

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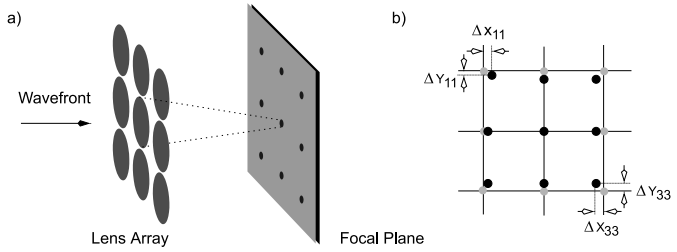

Fig. 1. a) The principle of Hartman-Shack wavefront detection and b) the focal point pattern of a reference wavefront (grey points) and of a distorted wavefront (black points)

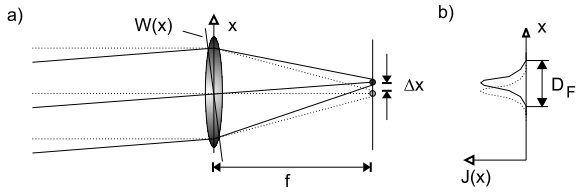

Fig. 2. a) The deviation of the focal point due to a wavefront tilt within the lens and b) the intensity distribution of a focal point

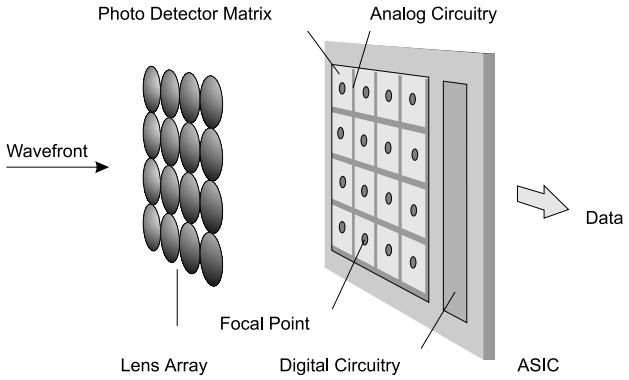

Fig. 3. The architecture of the system

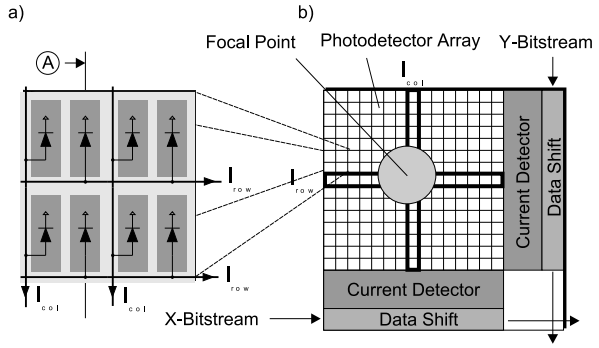

Fig. 4. a) A zoomed picture of the photo detectors within one cluster and b) the global architecture of one cluster

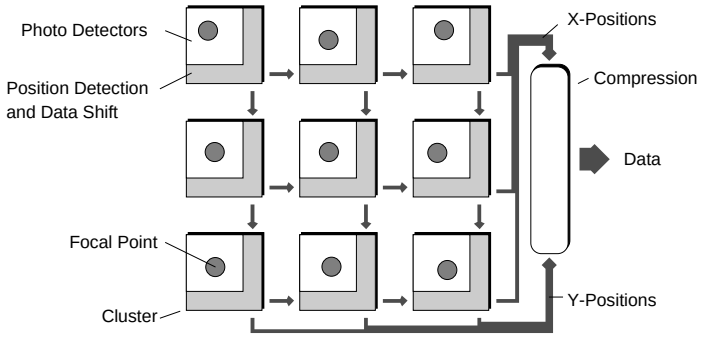

Fig. 5. The position detection clusters are linked together via shifting registers to push the position data to the compression unit

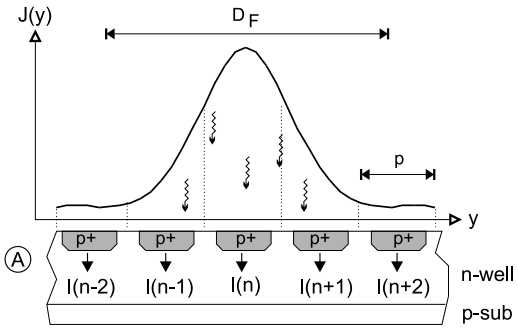

Fig. 6. The intensity distribution of a focal point, which is covering some photo diode stripes (not to scale)

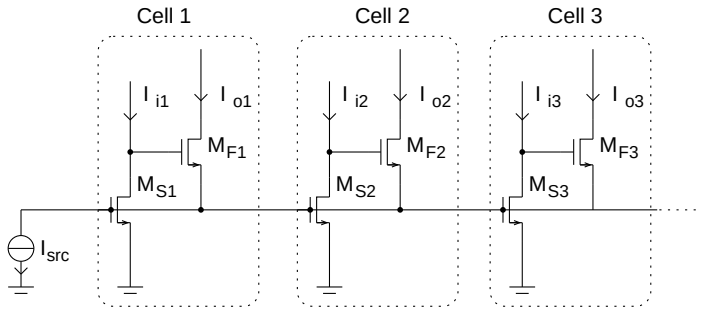

Fig. 7. The WTA topology presented with three NMOS-FET-WTA-cells.

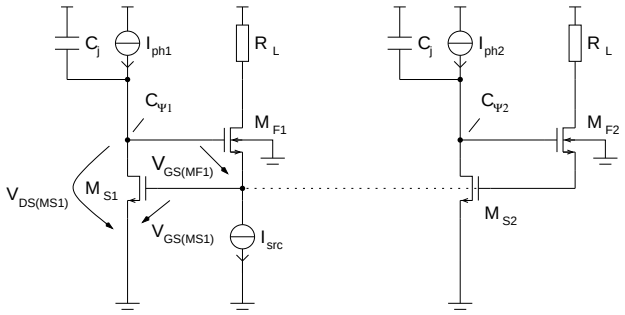

Fig. 8. The junction capacitors C_j of the photo diodes and the parasitic capacitors C_Ψ and C_Ψ reduce speed of transient response

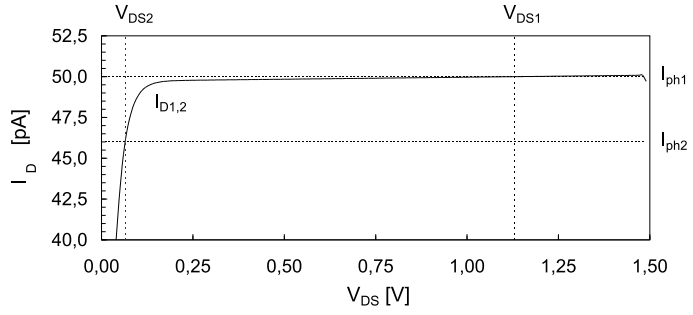

Fig. 9. An operating point calculation of two slightly differing input currents. $I_{D1,2}$ represents the subthreshold I_D vs. V_{DS} characteristic following eq. 4.

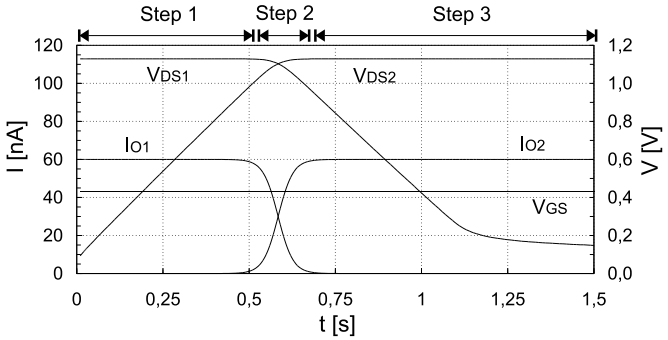

Fig. 10. The three timesteps in output current change (simulated data)

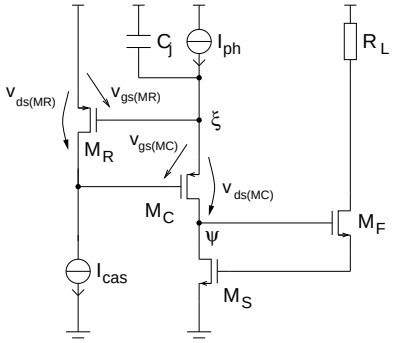

Fig. 11. Application of a regulated cascode to reduce the effect of the photo diodes' large junction capacitors

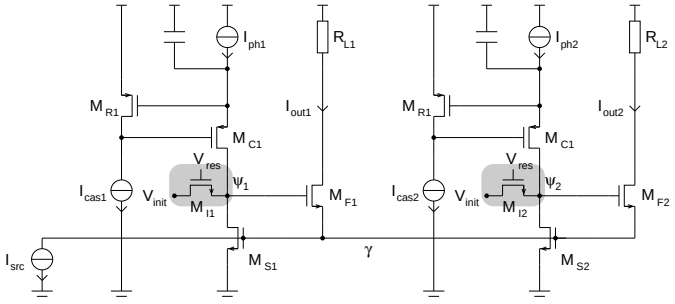

Fig. 12. Introduction of initial conditions for the drain voltages of M_S

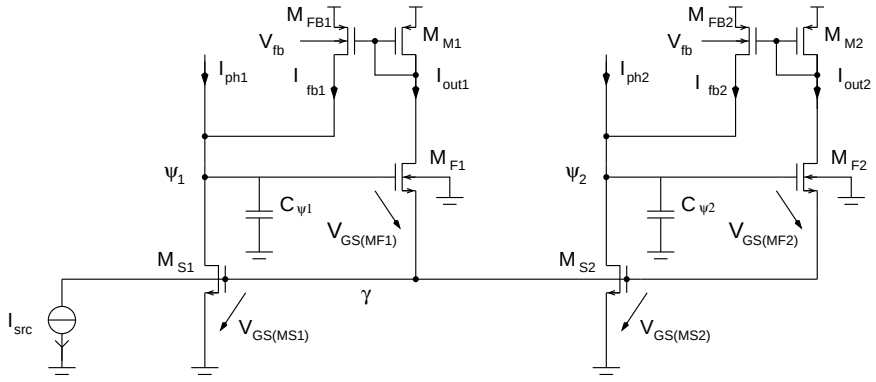

Fig. 13. The current mirror of M_{Mn} and M_{Fbn} mirrors the output current back to the input nodes

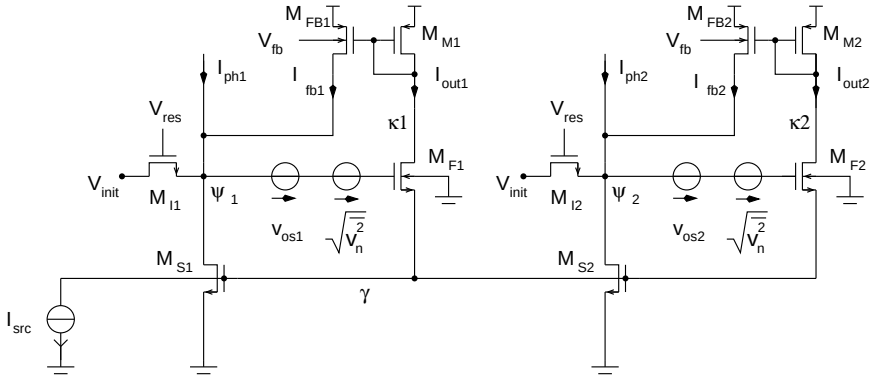

Fig. 14. Noise and mismatching considerations of a WTA-cell

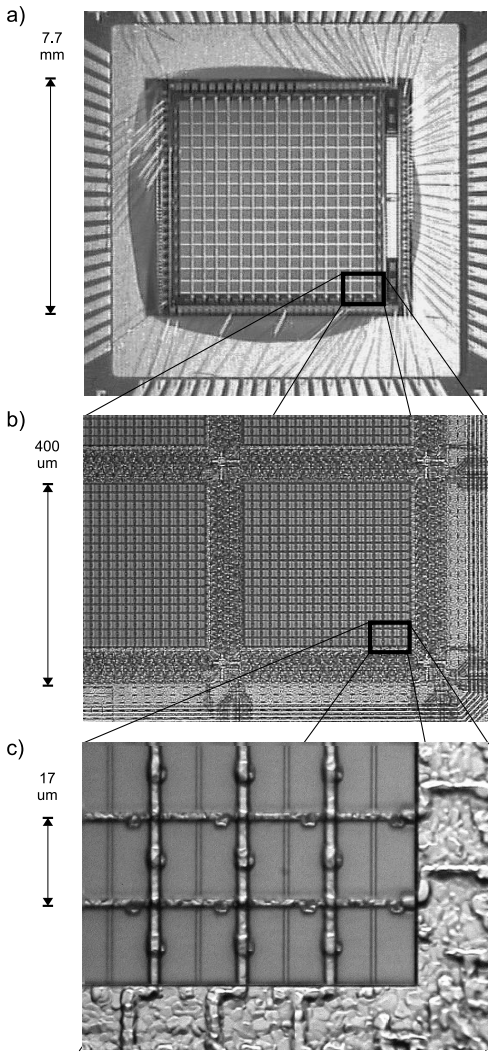

Fig. 15. A photography of the ASIC. Part a) shows the bonded die with an outline dimension of $7.7 \times 8.2\ mm^2$. Part b) is a zoomed section of the lowest right cluster of the 256 clusters for focal point position detection. Each cluster occupies an area of $400 \times 400\,\mu m^2$. In part c), a couple of photo diode pairs occupying an area of $17.6 \times 17.6\,\mu m^2$ each is enlarged. The whole ASIC includes 184000 photo diodes.

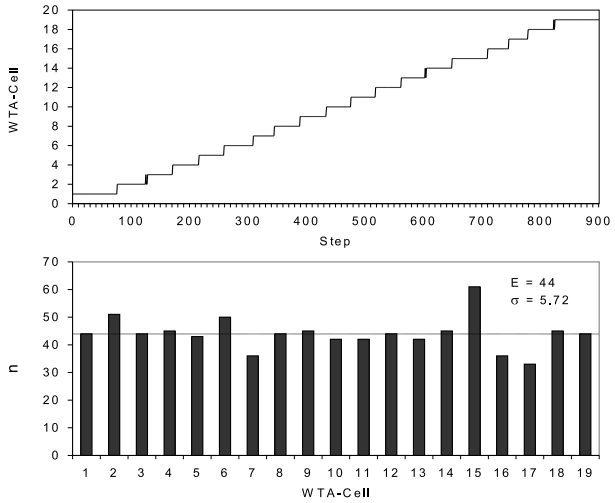

Fig. 16. $D_F = 17\mu m$, $P_F = 2\ nW$, no feedback

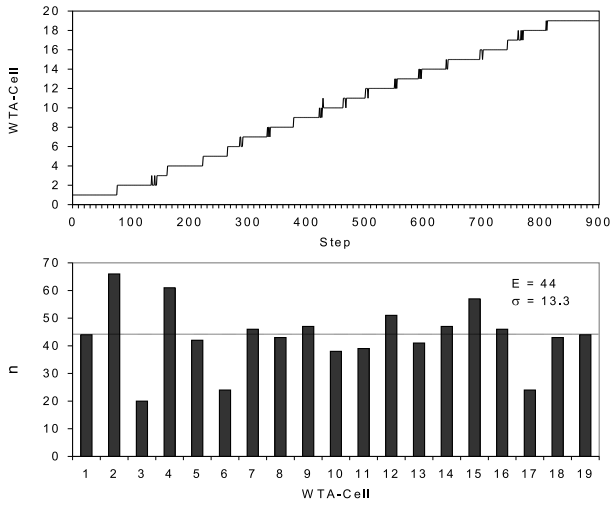

Fig. 17. $D_F = 17\mu m$, $P_F = 0.2\ nW$, feedback active

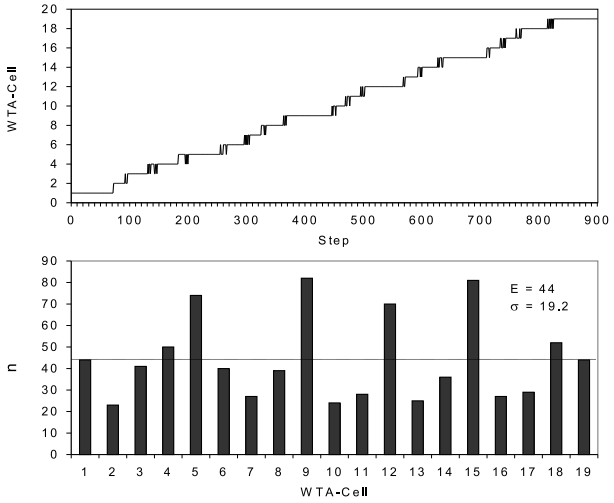

Fig. 18. $D_F = 180\mu m$, $P_F = 10\ nW$, no feedback

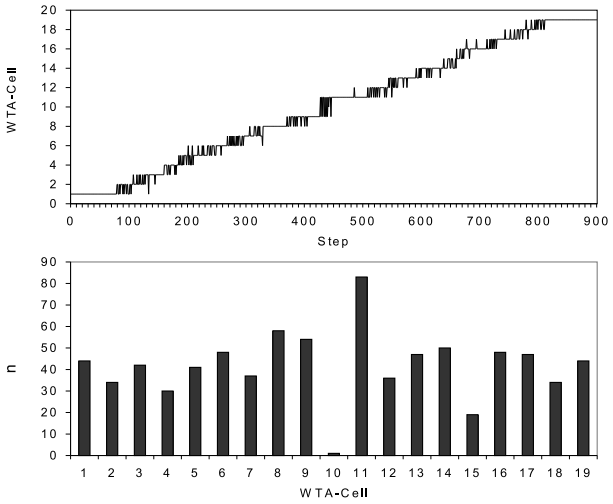

Fig. 19. $D_F = 180\mu m$, $P_F = 1\ nW$, feedback active

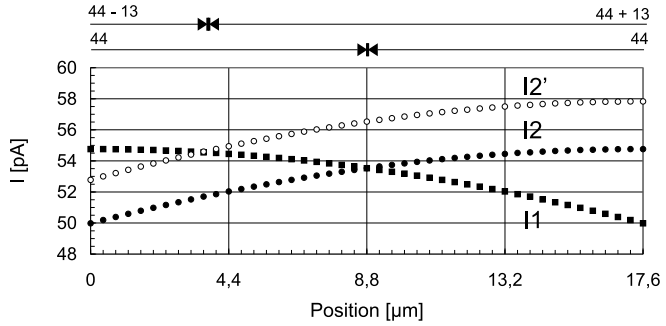

Fig. 20. Photo currents of neighbored cells versus position of movement (simulated data).

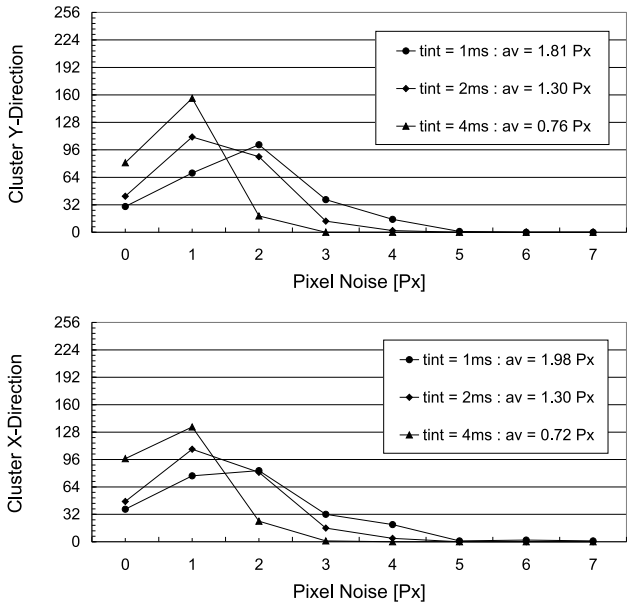

Fig. 21. Distribution of Pixel noise for X- and Y-Direction in units of Pixels

TABLE I

Measuring results for single spot measurements

Dir	$D_F[\mu m]$	$P_F[nW]$	σ_w	Feedback
x	17	2.0	7.0	no
y	17	2.0	5.9	no
x	17	0.2	13.9	yes
y	17	0.2	12.3	yes
x	180	10.0	26.1	no
y	180	10.0	29.8	no

TABLE II

Exemplary measuring results of optical glasses of spectacles

	Measurements Object I		
t_{int}	A_S $[D]$	A_C $[D]$	Θ_Z [°]
1 ms	0.262±0.012	1.184±0.051	82±1
2 ms	0.262±0.012	1.183±0.048	83±1
4 ms	0.270±0.012	1.169±0.041	84±1
specified	-0,25	-1.25	80
	Measurements Object II		
t_{int}	A_S $[D]$	A_C $[D]$	Θ_Z [°]
1 ms	0.715±0.012	0.131±0.059	-
2 ms	0.750±0.004	0.014±0.030	-
4 ms	0.754±0.004	0.004±0.021	-
specified	-0.75	0	0

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