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Master Thesis in Physics

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born in Stuttgart (Germany)

2026

ATLAS Tile Calorimeter

Trigger and Data Acquisition interface:

Level-0 Muon Signal Processing and Integration

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Abstract

The ATLAS experiment at CERN is undergoing the Phase-II Upgrade in preparation for the High-Luminosity LHC. As part of the new readout electronics for the Tile Calorimeter, the Trigger and Data Acquisition interface (TDAQi) module constructs trigger inputs for the Level-0 trigger systems within a strict latency budget of 250 ns. Signal processing and data transmission are implemented on an AMD Kintex UltraScale+ FPGA. This thesis describes the firmware development for the data path to the Level-0 Muon trigger. The TDAQi module receives digitized calorimeter data at 40 MHz, combines energy values and compares them against two defined thresholds. From this comparison, energy flags are generated which serve as trigger inputs and are transmitted to the Level-0 Muon trigger. Pipeline memories are implemented to store the muon data long enough for the Level-0 trigger to make a decision. Upon acceptance, the corresponding data is forwarded to the readout system. The trigger input generation and data transmission are validated.

Zusammenfassung

Das ATLAS-Experiment am CERN befindet sich im Phase-II-Upgrade zur Vorbereitung auf den High-Luminosity LHC. Als Teil der neuen Readout-Elektronik des Tile-Kalorimeters berechnet das TDAQi-Modul (Tile Calorimeter Trigger and Data Acquisition interface) die Triggereingaben für die Level-0-Trigger-Systeme unter Einhaltung eines strikten Latenzbudgets von 250 ns. Die Signalverarbeitung und Datenübertragung sind auf einem AMD Kintex UltraScale+ FPGA implementiert. Diese Arbeit beschreibt die Entwicklung der Firmware für den Datenpfad zum Level-0-Muon-Trigger. Das TDAQi-Modul empfängt Daten des Kalorimeters mit einer Rate von 40 MHz, summiert Energiewerte auf und vergleicht diese mit zwei Schwellenwerten. Aus diesem Vergleich werden Energie-Flags generiert, die als Triggereingaben dienen und an den Level-0-Muon-Trigger geschickt werden. Pipeline-Speicher werden implementiert, um die Muondaten bis zur Entscheidung des Level-0-Triggers zwischenspeichern. Wird ein Event akzeptiert, werden die zugehörigen Daten an das Readout-System weitergeleitet. Die Generierung der Triggereingaben sowie die Datenübertragung werden validiert.

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1 | Introduction

The discovery potential for rare processes and new physics is fundamentally constrained by the size of the available dataset. In collider experiments, the number of observed events scales with the integrated luminosity, which is the time integral of the instantaneous luminosity. To extend this reach, the High-Luminosity upgrade of the Large Hadron Collider (LHC) at CERN is being implemented during the ongoing collider shutdown. The HL-LHC is set to ultimately deliver an instantaneous luminosity of $L = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [1], an order of magnitude larger than the initial luminosity the accelerator could deliver. While this accelerates data collection, the increasing number of simultaneous proton-proton collisions poses a significant challenge for the experiments located at the LHC.

To ensure that it can maintain and even improve its physics performance despite the harsher conditions, the ATLAS experiment is undergoing its Phase-II Upgrade. The upgrade includes major changes to the detector, as well as the trigger and readout systems of the experiment.

The trigger system of ATLAS selects events with distinct characteristics to store them for physics analyses. The new Level-0 trigger is a hardware-based system that is implemented using custom electronics. Components across both detector readout and the Level-0 trigger systems have to comply with strict latency requirements. The hardware-based implementation ensures fast signal routing and data processing. The Level-0 trigger operates at the full bunch-crossing rate of 40 MHz and provides a trigger decision within $10 \mu\text{s}$.

As part of the Phase-II Upgrade, the on-detector and off-detector electronics of the Tile Calorimeter, which is the central hadronic calorimeter in ATLAS, will be replaced. Within the new readout chain, the Trigger and Data Acquisition interface (TDAQi) module connects the Tile Calorimeter electronics to the Level-0 trigger and the readout system. The TDAQi module receives energy measurements for every bunch crossing. Within a strict latency budget of 250 ns, it computes inputs for the Level-0 trigger systems, including

the Level-0 Muon trigger.

Tile Calorimeter data is used by the Level-0 Muon trigger systems to reject background events by enforcing a coincidence requirement. Signals created by non-prompt muons, which do not originate from the primary collision, are suppressed through this veto. The coincidence requirement with the Tile Calorimeter measurements was implemented for specific detector regions during the last data-taking period at ATLAS and significantly reduced muon trigger rates [2].

The signal processing path for the L0Muon trigger in the firmware of the TDAQi module is presented in this thesis. The module generates energy flags from threshold comparisons. Specifically, adjacent cells are combined and compared against two thresholds, one for isolated muons and one for muons in proximity to a jet. Copies of the energy flags are buffered and transmitted to the readout system if the Level-0 trigger accepts the corresponding event.

This thesis is structured in the following way: Chapter 2 introduces the LHC and the ATLAS experiment. In Chapter 3, the Phase-II Upgrade is presented, focusing on the changes to the trigger and data acquisition architecture and to the Tile Calorimeter readout chain. Chapter 4 provides an overview of the Tile Calorimeter PreProcessor and TDAQi modules. The firmware of the TDAQi is discussed in Chapters 5 and 6, respectively. Chapter 5 covers the real-time generation of trigger inputs and the data transmission to the Level-0 trigger, while Chapter 6 discusses the buffering of data and transmission to the readout system. While a general overview of the firmware is presented, the focus of both chapters remains on the L0Muon data path. Firmware validation procedures are described in Chapter 7. Chapter 8 summarizes the results and presents an outlook.

Author's Contribution

The development of the Trigger and Data Acquisition interface (TDAQi) module is an ongoing, multi-year project involving multiple developers. The work presented in this thesis benefits heavily from previous and ongoing development of the hardware, but also the firmware design of the module.

At the outset of this project, the general architecture of the firmware was established and several modules were implemented already. The author's contribution to the firmware is the development, integration and testing of the Level-0 Muon trigger (L0Muon) data path. This includes the logic to generate the trigger inputs, in particular the generation of muon sums and the threshold comparison. While the transmission logic was already in place, the data-frame construction was implemented by the author.

In the readout part of the firmware, the muon data path was integrated by the author alongside existing readout pipelines. Designated memory resources were allocated and missing FIFO buffers in the derandomizer module were added. The state machine controlling the transmission to the readout system was modified to incorporate the muon data into the data packet.

The author designed and implemented the validation software detailed in the thesis. The validation tests were conducted using the test setup located at the Kirchhoff Institute for Physics in Heidelberg. The transmission and latency measurements were also performed using this infrastructure, with a pre-existing firmware configuration for the Tile Rear Extension (TREX) module.

2 | The ATLAS Experiment at the LHC

The Large Hadron Collider (LHC) [3] at the European Organization for Nuclear Research (CERN) is the largest particle accelerator in the world. It is situated in a tunnel with a circumference of 27 km, located beneath the Franco-Swiss border. The ATLAS experiment is one of the four major experiments at the LHC.

This chapter gives a short overview of the LHC and outlines the High Luminosity Large Hadron Collider (HL-LHC) Upgrade. The main subsystems of the ATLAS detector and the Trigger and Data Acquisition (TDAQ) architecture are described, as operated during the most recent data-taking period.

2.1 The Large Hadron Collider

The LHC accelerates two beams of protons or heavy ions traveling in opposite directions. The beams collide at four interaction points, where the major experiments are located. Two of them, ATLAS [5] and CMS [6], are designed as general-purpose detectors. The ALICE experiment [7] specializes in the study of heavy-ion collisions. The LHCb experiment [8] was designed to study flavor physics, focusing on CP-violating processes and rare decays. A schematic view of the LHC with the four main experiments is shown in Figure 2.1.

The two proton beams are structured into bunches. A full orbit of the LHC consist of 3564 bunches, although in operation not all bunch slots are filled with particles. Each collision slot is assigned a Bunch Crossing Identifier (BCID) value from 0 to 3563.

The instantaneous luminosity L of the LHC can be derived from the parameters of the machine. Assuming a Gaussian beam distribution and equal beams, it is defined as:

$$L = \frac{f_{\text{orbit}} \cdot n_b \cdot N_b^2}{4\pi \cdot \sigma_x \cdot \sigma_y}. \quad (2.1)$$

Here, f_{orbit} denotes the orbit frequency, N_b the number of particles per colliding bunch, and n_b the number of filled bunches. The beam widths in the x and y direction at time of

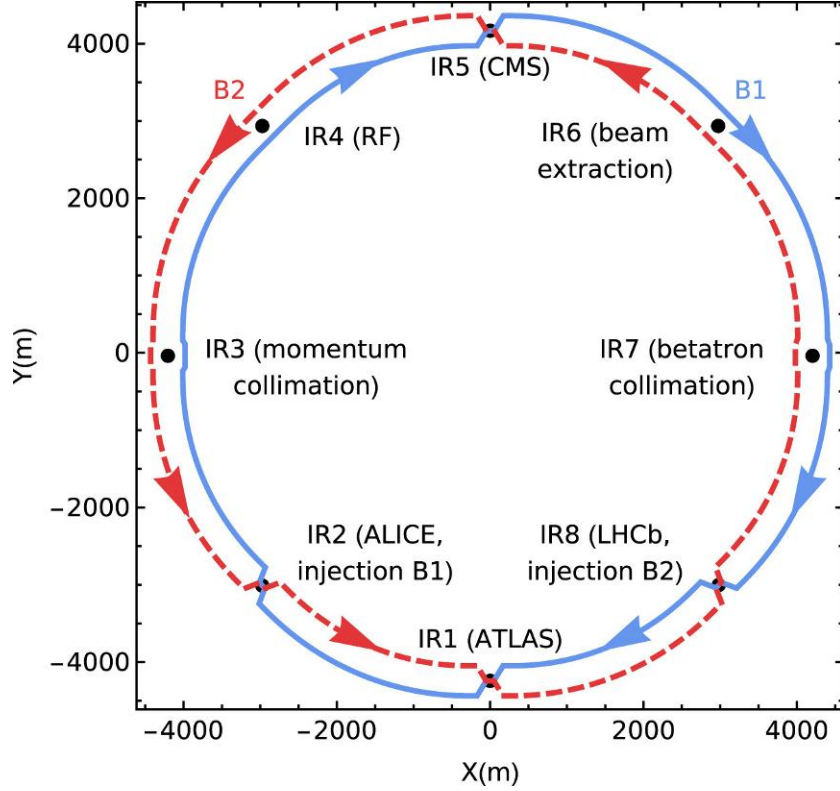


Figure 2.1: Schematic of LHC with the four experiments ATLAS, LHCb, CMS, and ALICE [4]. The beam separation is exaggerated.

the collision are denoted by σ_x and σ_y , respectively [9].

The integrated luminosity $\mathcal{L}_{\text{int}}$ is the instantaneous luminosity integrated over time:

$$\mathcal{L}_{\text{int}} = \int L dt. \quad (2.2)$$

The larger the integrated luminosity of an accelerator, the higher the total number of interactions.

The LHC began operation in 2010, delivering proton collisions at a center-of-mass energy of up to $\sqrt{s} = 8$ TeV. During the first data-taking period, referred to as Run 1, the peak luminosity was $L = 7.7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ [10]. After the first Long Shutdown (LS) of the accelerator from 2013 to 2015, the center-of-mass energy was increased to 13 TeV [11]. The machine delivered an instantaneous luminosity of up to $L = 1.9 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [12] during Run 2, which concluded prior to LS 2 in 2018. The LHC commenced operation in 2022 for Run 3 with a center-of-mass energy of $\sqrt{s} = 13.6$ TeV and a maximum instantaneous luminosity of $L = 2.61 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [13].

On 29 June 2026, the LHC entered its current upgrade period, LS 3 [14]. During LS 3, major modifications to the accelerator are implemented to significantly increase its luminosity. Run 4 is set to begin in 2030, marking the start of operation for the HL-LHC.

2.1.1 The High-Luminosity Upgrade

The LHC is set to undergo major changes during the collider shutdown, referred to as the High-Luminosity Upgrade [15]. Simultaneously, the experiments at the LHC will receive upgrades to cope with the increase in luminosity.

The HL-LHC project aims to achieve an instantaneous luminosity of up to $L = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [1]. This would result in an integrated luminosity of 300–400 fb^{-1} per year. The goal of the project is to deliver a total integrated luminosity of 4000 fb^{-1} by the early 2040s. For comparison, the LHC has delivered an integrated luminosity of 536 fb^{-1} [16] over the duration of its first three runs (2010–2026).

The larger dataset will allow for more precise measurements of Standard Model parameters, such as the properties of the Higgs boson, as well as increase the sensitivity for Beyond the Standard Model (BSM) physics searches.

2.2 The ATLAS Detector

The ATLAS experiment [5, 17] is a general-purpose particle detector sensitive to a wide range of physics.

Data taking at the experiment began in Run 1 in 2010. The increasing luminosity of the LHC motivated the Phase-I Upgrade of the detector, which took place during LS 2. During LS 3, another series of changes to the detector as well as to the trigger and readout systems, collectively called the Phase-II Upgrade, are being implemented to prepare the ATLAS experiment for the HL-LHC.

Figure 2.2 shows a cutaway view of the ATLAS detector. The detector is cylindrical, 44 m long and 25 m in diameter, with a central barrel flanked by two disk-shaped endcaps. The ATLAS detector consists of several subsystems arranged concentrically around the beamline.

The coordinate system used to describe the detector defines the z -axis in direction of the

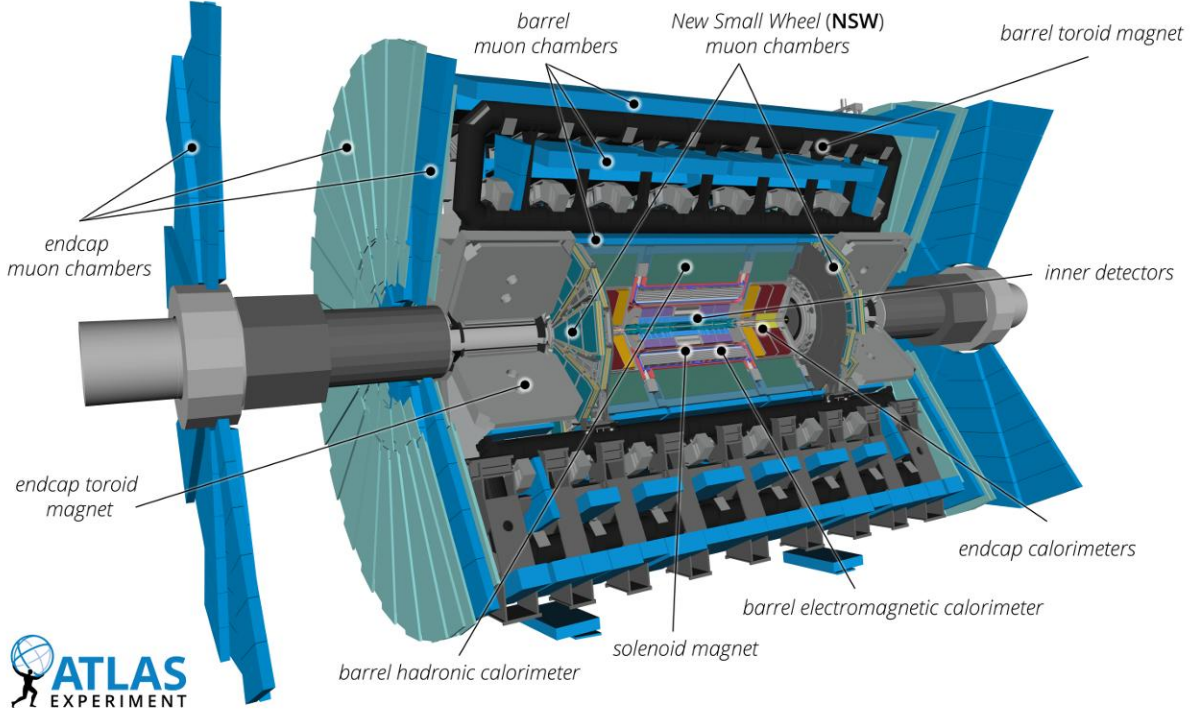


Figure 2.2: Cutaway view of the ATLAS detector. Taken from [17].

beam, with the point of origin being the nominal collision point. The polar angle θ is the angle to the z -axis, while the azimuthal angle ϕ is defined in the transverse plane. Instead of θ , the pseudorapidity η is commonly used. It is defined as:

$$\eta = -\ln \tan \frac{\theta}{2}. \quad (2.3)$$

2.2.1 Detector Systems

The Inner Detector (ID) provides particle tracking coverage in the region $|\eta| < 2.5$. It consists of three subsystems; the Pixel Detector, the Semiconductor Tracker (SCT), and the Transition Radiation Tracker (TRT). The Pixel Detector, which is closest to the beam line, consists of layers of silicon pixels and typically provides four measurements for each track. After that, particles pass eight layers of silicon sensor strips in the SCT. The TRT, which measures transition radiation using drift tubes, forms the outermost layer of the ID.

The ID is immersed in a magnetic field of up to 2 T, created by a solenoidal magnet. The deflection of charged particles in this magnetic field is used when reconstructing their charge and momentum.

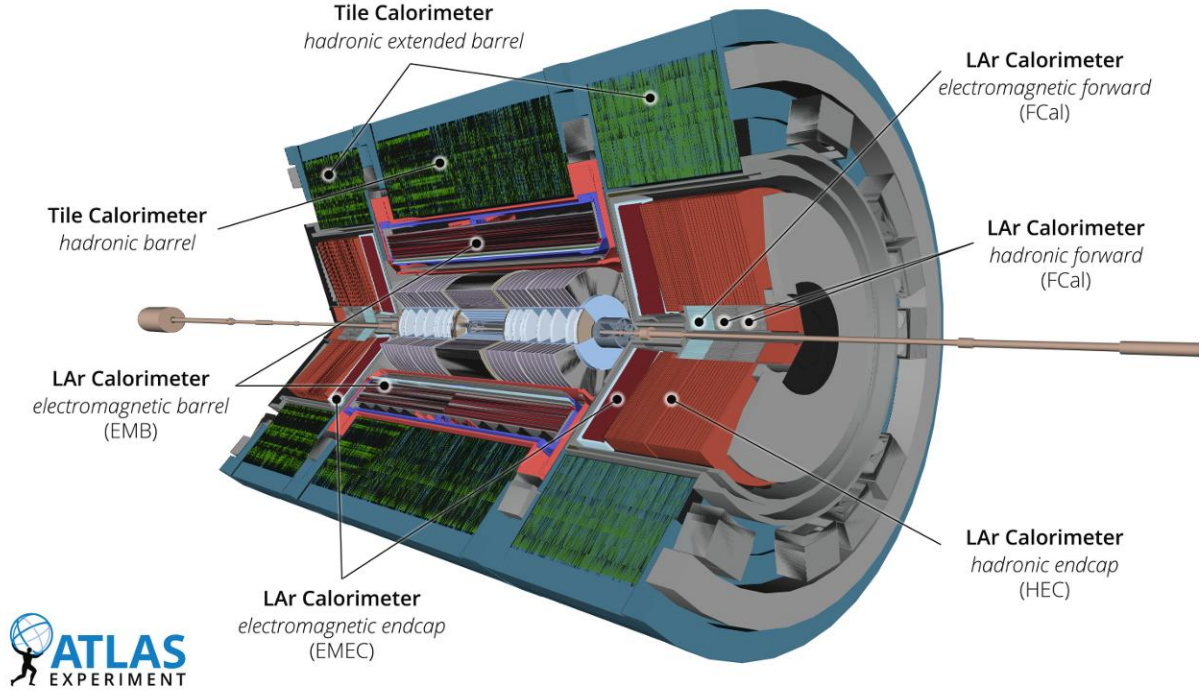


Figure 2.3: Cut-away view of the calorimetry system of the ATLAS detector. Taken from [17].

Surrounding the solenoid is the calorimetry system of the ATLAS detector, consisting of the Liquid Argon (LAr) calorimeters and the Tile Calorimeter. An image of this system is presented in Figure 2.3.

The LAr calorimeters are sampling calorimeters that use liquid argon as the active material. For electromagnetic calorimetry, the central barrel, which uses lead absorbers, is extended on each side by an endcap module made of the same material.

The Tile Calorimeter is the central hadronic calorimeter in the ATLAS detector. It is a sampling calorimeter consisting of plastic scintillating tiles and steel absorbers. As shown in Figure 2.3, the Tile Calorimeter is segmented into a central barrel and two extended barrels, covering a region of $|\eta| < 1.6$. The range for hadronic calorimetry is extended by two LAr endcaps with copper as the passive material.

Two forward LAr calorimeters on each side, one electromagnetic and one hadronic, cover the area closest to the beam line. The forward modules feature copper and tungsten absorbers, respectively.

After passing through the electromagnetic and hadronic calorimeters, minimum-ionizing

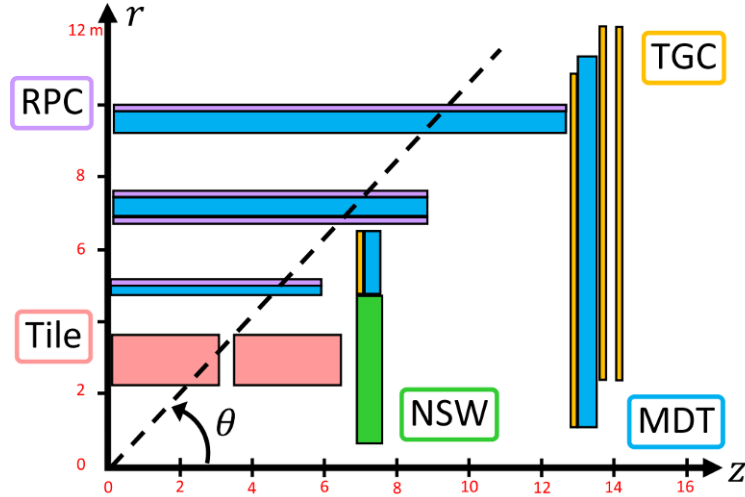


Figure 2.4: Schematic view of the MS subsystems and the Tile Calorimeter. Taken from [18].

muons can be detected in the Muon Spectrometer (MS), which constitutes the outermost layers of the ATLAS detector. Different detector technologies are employed to identify muon candidates and reconstruct their tracks. Figure 2.4 presents a schematic side-view of the MS and the Tile calorimeter. Three systems of superconducting air-core toroid magnets, one surrounding the barrel and one at each endcap, create a magnetic field in the MS, which curves the muon trajectories, allowing for momentum reconstruction. The toroid magnets are marked in the image in Figure 2.2.

In the barrel sector, Monitored Drift Tube (MDT) chambers, arranged in three layers, provide measurements in the pseudorapidity region $|\eta| < 1.3$. Resistive Plate Chambers (RPCs) are implemented for triggering and span the same acceptance range. In the endcap region, covering $1.05 < |\eta| < 2.7$, MDTs provide precision tracking and are complemented by Thin Gap Chambers (TGCs), which provide fast signals for triggering as well as supplementary tracking information.

The New Small Wheel (NSW), which was implemented as part of the Phase-I Upgrade, is positioned directly next to the calorimeters, as shown in Figure 2.2. It features small-strip TGCs as well as micro-mesh gaseous structure (Micromegas) detectors and covers a range of $1.3 < |\eta| < 2.7$. The NSW information is used by the muon trigger to improve background rejection by applying a coincidence veto, which filters out particles that do not originate from the collision. In the pseudorapidity range of $1.05 < |\eta| < 1.3$, which is not covered by the NSW, signals in the outermost layer of the Tile Calorimeter are used

instead.

The schematic view presented in Figure 2.4 illustrates this coincidence. Particles originating from the collision point (shown as the origin in the figure) are expected to traverse the NSW or the Tile Calorimeter. Consequentially, muon candidates in the corresponding pseudorapidity ranges are rejected if there is no coinciding energy deposit detected in these systems.

2.2.2 Trigger and Data Acquisition

Bandwidth and storage constraints limit the amount of collision data that can be permanently recorded. To ensure that events of physics interest are stored for offline analysis, those with distinctive signatures must be identified. This event selection is realized by the trigger system.

The Run 3 trigger system [17] consists of a hardware-based Level-1 trigger, and a second-level software trigger, the High-Level Trigger (HLT).

The Level-1 trigger is composed of a number of subsystems, implemented on custom electronics. The Level-1 Calorimeter trigger (L1Calo) identifies physics objects in the calorimetry system, such as high-energy electrons, photons, or jets. It comprises specialized modules, called the jet Feature EXtractor (jFEX), electron Feature EXtractor (eFEX), and global Feature EXtractor (gFEX), each employing selection algorithms tailored to specific objects. The FEXs are implemented on custom hardware modules which will be reused in the Phase-II version of the trigger system. Muon signatures are identified by the Level-1 Muon trigger (L1Muon), which processes data from the MS subsystems and the Tile Calorimeter. The Level-1 Topological trigger (L1Topo) performs topological selection with the information from the L1Calo and L1Muon triggers.

The final Level-1 trigger decision is made by the Central Trigger Processor (CTP) based on the L1Calo, L1Muon, and L1Topo inputs. The maximum latency for the Level-1 trigger is $2.5\,\mu\text{s}$, while the maximum output rate is 100 kHz.

When a trigger decision is made, the data from the subsystems is forwarded to the readout system. The full event is assembled and transmitted to the HLT, which is a software-based trigger operated on a commercial server farm. The HLT executes a series of reconstruction

and selection algorithms to further process the event and reach a final trigger decision. It reduces the final event rate to 1 kHz. If the HLT accepts an event, the corresponding data is moved to permanent storage.

3 | The Phase-II Upgrade

As the instantaneous luminosity of the LHC increases, the number of interactions per bunch crossing rises. In Run 3, the average number of interactions was $\langle\mu\rangle = 56$ [19]. For HL-LHC, up to $\langle\mu\rangle = 200$ [1] interactions per bunch crossing are expected. These collisions, which occur in addition to the collision of interest, are referred to as pile-up. The high pile-up, high-radiation environment of HL-LHC presents a challenge to detector systems, as well as trigger and readout electronics.

The Phase-II Upgrade [20] comprises a number of changes scheduled to be implemented during LS 3, which are designed to prepare the ATLAS experiment for the conditions of HL-LHC.

This chapter presents a general overview of the Phase-II Upgrade of the ATLAS experiment. The new design of the TDAQ system and the upgrade of the readout electronics for the Tile Calorimeter are discussed in more detail.

3.1 General Overview

To maintain the tracking performance of ATLAS in the high pile-up conditions of HL-LHC, the ID will be replaced. The new Inner Tracker (ITk) [21] is an all-silicon detector, with pixel layers surrounded by layers of strip detectors. The ITk offers improved granularity, while also being more resistant to radiation. The coverage of the ITk is extended from $|\eta| < 2.5$ up to $|\eta| < 4$.

For both the LAr and Tile calorimeters, a full replacement of the readout electronics is foreseen, while the detectors themselves remain mostly unchanged [22, 23]. The upgrade is necessary because the electronics currently in use cannot meet the data throughput and latency requirements of the upgraded TDAQ system. Furthermore, with the rising luminosity, the radiation hardness of the readout system becomes a much bigger concern. Many of the current electrical components would not withstand the radiation dose expected over the duration of HL-LHC. Finally, some of the electronics were designed and built over

20 years ago and maintaining them becomes challenging and expensive, as replacement components are no longer available.

The Phase-II Upgrade of the MS [24] includes the installation of new RPCs in the barrel region to increase the rate capability. Changes to the TGCs in the endcap region are planned to enhance the granularity and tighten coincidence requirements to reduce the rate of fake muon triggers. Additionally, a large part of the readout electronics will be replaced to ensure compatibility with the upgraded TDAQ system.

The high pile-up environment of HL-LHC presents a significant challenge to the TDAQ system of ATLAS [25]. Trigger selectivity needs to be maintained while keeping the low energy thresholds used previously to preserve sensitivity at lower energies. To achieve this, the maximum trigger rate is raised and the latency budget for the trigger is increased to allow for the implementation of more complex selection algorithms. The Phase-II TDAQ system represents a redesign of the previous TDAQ architecture, featuring new trigger and readout hardware.

3.2 Phase-II Upgrade of the ATLAS TDAQ System

The Phase-II TDAQ system [25, 26] is designed to operate under HL-LHC conditions while maintaining the acceptance range of previous runs. The design of the Phase-II TDAQ architecture is pictured in Figure 3.1.

Like the Run 3 configuration, the Phase-II trigger system consists of two processing stages. The hardware-based first-level trigger is called the Level-0 trigger, a second-level software trigger is called the Event Filter.

The Level-0 trigger operates at the collision rate of the LHC, which is 40 MHz. It is capable of an acceptance rate of 1 MHz, compared to the maximum rate of 100 kHz in the Phase-I first-level trigger system, which is described in Chapter 2.2.2. The latency budget of the first-level trigger is extended from $2.5\ \mu\text{s}$ to $10\ \mu\text{s}$ compared to the previous configuration.

If the Level-0 trigger system selects an event for further processing, it issues the Level-0 Trigger Accept (L0A) signal, which initiates the data readout across all subdetectors. Data acquisition is coordinated by the Front-End Link eXchange (FELIX) system and the data handlers. The Dataflow system assembles the data into a full event, before it is

transmitted to the Event Filter.

The Event Filter is a software-based trigger that is operated on a commodity processor farm. It reduces the rate from 1 MHz to 10 kHz, which is the final data collection rate. By comparison, the Phase-I system had a data collection rate of around 2 kHz.

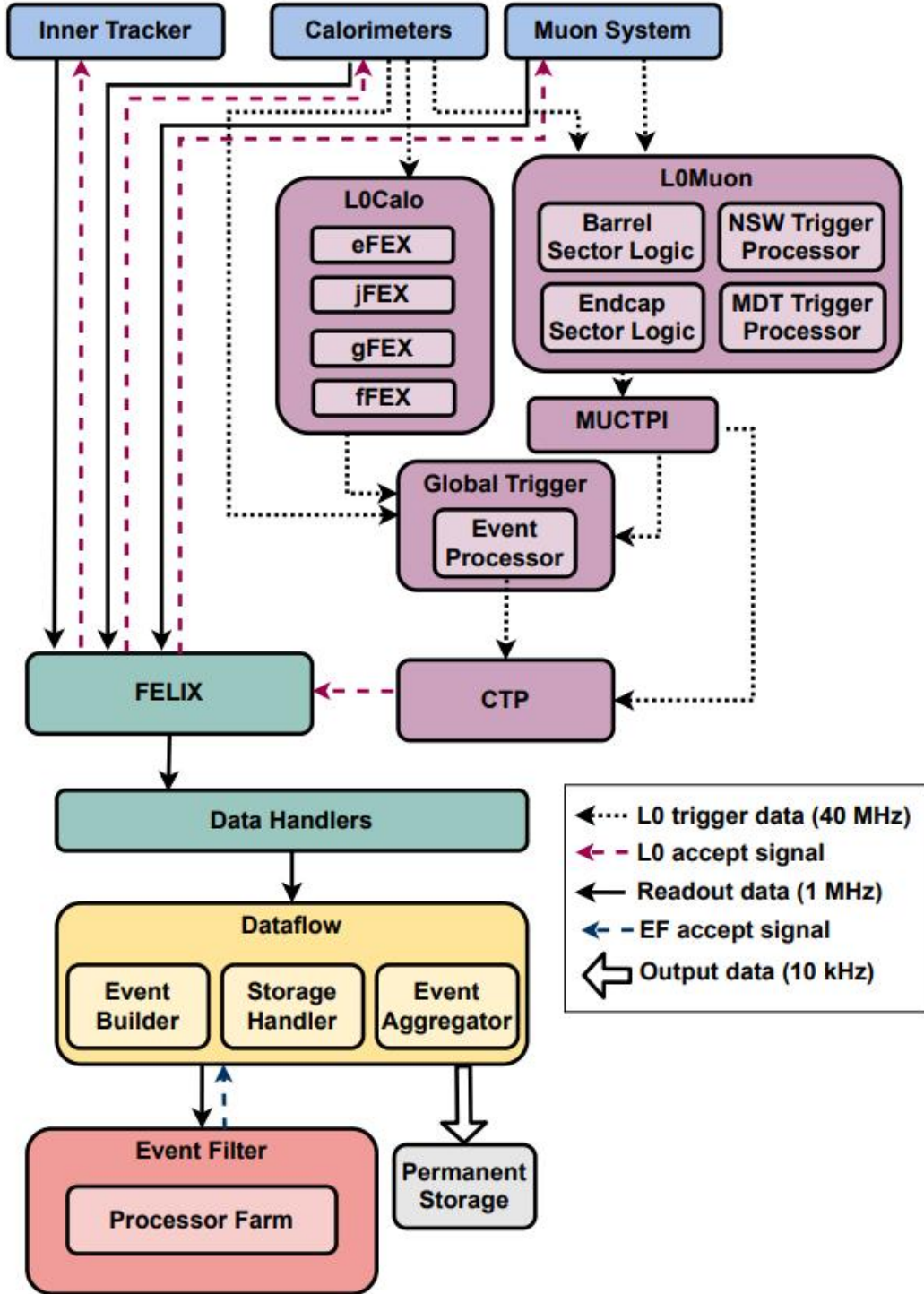


Figure 3.1: Phase-II Design of ATLAS TDAQ architecture. Taken from [27].

3.2.1 The Level-0 Trigger System

The Level-0 trigger serves as the new first-level trigger of the ATLAS experiment. The Level-0 Calorimeter trigger (L0Calo) and Level-0 Muon trigger (L0Muon) construct trigger objects in localized detector regions, which are then refined and combined by the Global trigger. The Central Trigger Processor (CTP) issues the final trigger decision.

The L0Calo trigger is implemented through dedicated modules, each optimized for the identification of specific calorimeter signatures. The electron Feature EXtractor (eFEX) identifies electrons, photons, and τ -leptons; the jet Feature EXtractor (jFEX) reconstructs τ -leptons, jets and the missing transverse energy E_T^{miss} ; while the global Feature EXtractor (gFEX) processes large-area jets and performs additional E_T^{miss} computations. The forward Feature EXtractor (fFEX) focuses on the identification of jets and electrons in the forward direction. The L0Calo trigger is based on the Run 3 L1Calo trigger. The jFEX, eFEX and gFEX hardware modules are retained and deployed with updated firmware.

Using trigger inputs from the upgraded MS and the Tile Calorimeter, the L0Muon trigger reconstructs tracks and identifies muon candidates. The system comprises two Sector Logic (SL) boards [18] alongside dedicated NSW and MDT Trigger Processors. The Barrel Sector Logic (BSL) receives inputs from the RPC and MDT modules in the barrel region as well as from the Tile Calorimeter, while the Endcap Sector Logic (ESL) receives data primarily from the detectors in the endcap region, including the extended barrels of the Tile Calorimeter.

Tile Calorimeter and NSW measurements are used to enforce a coincidence veto, similar to the Run 3 implementation, which was described in Chapter 2.2.2. The upgraded L0Muon trigger receives information across the full Tile Calorimeter coverage, as the rejection of fake muons is critical in the high pile-up HL-LHC conditions. A comprehensive overview of the Tile Calorimeter trigger inputs is provided in Chapter 5.1.1.

The Global trigger uses the information from the L0Calo and L0Muon triggers as well as high-granularity calorimeter data. It combines and refines the trigger objects from the other systems, using offline-like algorithms. The final component of the Level-0 trigger is the CTP, which takes the final L0A decision based primarily on information from the Global trigger but also the other trigger systems.

3.2.2 Readout and Dataflow Systems

Following a Level-0 trigger decision, the L0A signal is routed to the detector subsystems to initiate the readout process. The event data is assembled by the Dataflow system and transmitted to the Event Filter.

The FELIX system [28] is a key component of the detector readout. The system relays Timing, Trigger and Control (TTC) signals to the respective front-end electronics of the ATLAS subdetectors and routes data fragments to the readout system.

The FELIX system is implemented as custom Peripheral Component Interconnect express (PCIe) cards which are hosted on commercial servers. It was implemented for some detector and trigger systems as part of the Phase-I Upgrade. For Phase-II, the system will provide the interface between data acquisition, TTC systems, all trigger systems and the front-end electronics of all subdetectors.

The Dataflow system collects the data fragments from the different systems to assemble the full event. It buffers the results before they are transmitted to the Event Filter. After the Event Filter decision, the Dataflow system sends the relevant event data to permanent storage.

3.3 Phase-II Upgrade of the Tile Calorimeter

With the Phase-II Upgrade, the entire readout electronics of the Tile Calorimeter will be replaced while the detector itself will remain largely unchanged [22]. The Phase-II readout electronics for the calorimeter are designed to cope with the high pile-up and high-radiation environment of the HL-LHC and to fulfill the requirements of the Phase-II ATLAS TDAQ architecture. Especially in the on-detector electronics, components with a high radiation tolerance are used. The new system is more mechanically accessible, allowing for easier installation and maintenance. Additionally, the new readout electronics are structured into smaller independent units than before. This modularity makes the system more reliable and mitigates the impact of a component failure.

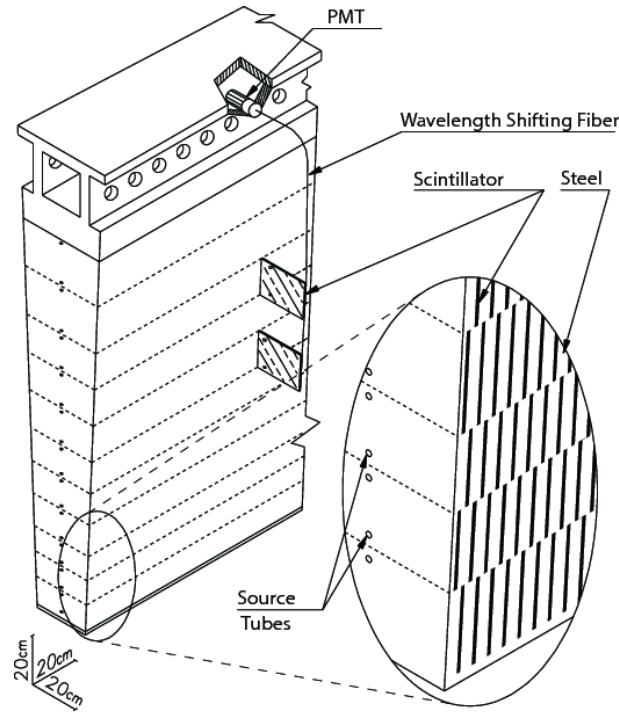


Figure 3.2: Tile Calorimeter wedge module [22]

3.3.1 Specifications of the Tile Calorimeter

The Tile Calorimeter is a sampling calorimeter made of plastic scintillating tiles and steel absorbers. It consists of one central barrel and two extended barrels, one on each side [29]. Figure 2.3 presents a generated view of the calorimetry system that shows the different barrels. Each of the barrels is divided into 64 wedge-shaped modules, with an azimuthal coverage of $\Delta\phi = 0.1$. Figure 3.2 shows a sketch of one of these modules.

The photons produced by the scintillators are collected using wavelength-shifting fibers. The fibers are grouped together, which creates the segmentation of the calorimeter into cells. Photomultiplier Tubes (PMTs) are used to convert the photons into electrical signals. Each cell is read out by two PMTs. In total, the Tile Calorimeter features ~ 10000 PMTs.

Figure 3.3 shows a schematic of the Tile Calorimeter cell segmentation. Radially, the calorimeter is segmented into three layers (A , BC or B , D). A system of scintillators between the central and extended barrels is used to detect energy escaping the electromagnetic calorimeter ($E1$ - $E4$).

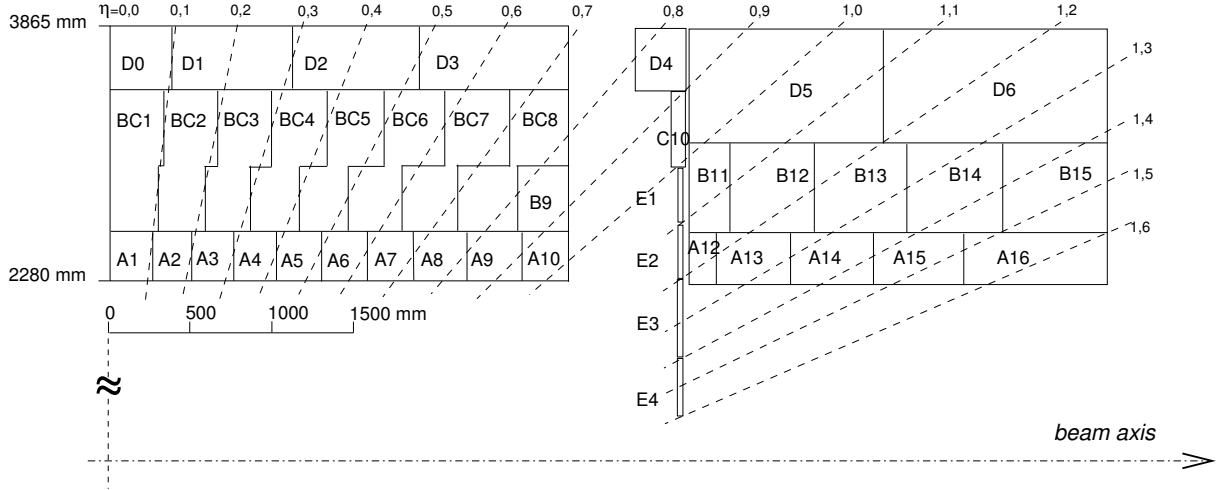


Figure 3.3: Map of Tile Calorimeter cells. The central barrel segmentation is shown on the left, the extended barrel segmentation on the right. Taken from [22].

3.3.2 The Phase-II Readout chain

The Phase-II readout architecture for the Tile Calorimeter [30] is illustrated in Figure 3.4. The system comprises on- and off-detector components. The on-detector electronics are situated directly on the calorimeter modules, whereas off-detector components are placed in an electronics service cavern, about 100 m away from the detector.

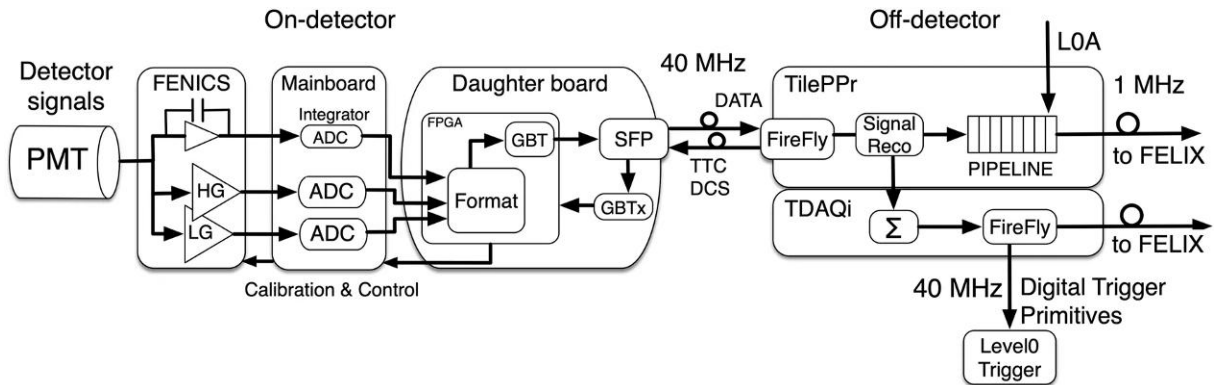


Figure 3.4: Schematic diagram of the upgraded Tile Calorimeter readout chain. Taken from [31].

The on-detector electronics are designed to be highly modular. They are housed in mechanical containers called mini-drawers, each of which processes signals from 12 PMTs. These drawers operate independently in terms of power and cooling.

The Front End board for the New Infrastructure with Calibration and signal Shaping (FENICS) is the first component of the readout chain. For each PMT, one of these boards

shapes and amplifies the signal using two different gain settings. Additionally, these boards are capable of current integration, which is used for calibration procedures and to monitor the luminosity.

Each mini-drawer features one Mainboard and one Daughterboard. On the Mainboard, the analog signals from the PMTs are digitized by 12-bit Analog-to-Digital Converters (ADCs). For the current integration signal, the board features an additional 14-bit ADC. The dynamic ranges of the ADCs and the dual-gain amplification ensure that cell energies between 5 MeV and 5 TeV can be measured.

The Daughterboard handles the communication with the off-detector electronics through optical links. Each Daughterboard provides four links, each with a transmission rate of 9.6 Gbps, to transfer detector data to the counting room. The board also hosts two downstream links which relay TTC signals to the on-detector components, each operating at 4.8 Gbps.

The data is sent to the off-detector electronics at the bunch-crossing frequency of 40 MHz. The total transmission rate from the on-detector electronics to the counting room is 40 Tbps.

The Tile PreProcessor (TilePPr) module [32] forms the core component of the off-detector electronics. It processes signals from the on-detector components, provides trigger inputs for the Level-0 trigger systems, and buffers event data until the L0A signal is issued. The TilePPr module is presented in Chapter 4.1.

4 | The TilePPr and the TDAQi

For each bunch crossing, the on-detector electronics of the Tile Calorimeter send digitized data to the TilePPr module, located off-detector in a support cavern [32]. The module performs energy reconstruction and calibration in real-time, providing trigger inputs to the Level-0 trigger systems at 40 MHz. In addition, it features pipeline memories to store data samples which can be extracted and transmitted to the FELIX system if the L0A is issued.

This chapter provides an overview of the TilePPr module and its components. The Compact Processing Module (CPM) and ATCA Carrier Base Board (ACBB) are introduced, followed by a physical description of the TDAQi module and an outline of its firmware design.

4.1 The Tile PreProcessor

The TilePPr module is based on the Advanced Telecommunications Computing Architecture (ATCA) standard. Each TilePPr consists of four CPMs, an ACBB and a TDAQi module. The entire calorimeter is read out by 32 TilePPr modules situated in four ATCA shelves. Each module covers an area of 1.6×0.4 in the $\eta - \phi$ plane. The image in Figure 4.1 shows the TilePPr module.

4.1.1 The Compact Processing Module

Each of the 32 TilePPr modules features four CPMs, requiring 128 CPMs to cover the entire calorimeter. Each CPM can process signals from two modules of the Tile calorimeter, consisting of 37 calorimeter cells. In the $\eta - \phi$ plane, this corresponds to an area of 1.6×0.1 .

The CPMs receive the calorimeter data from the on-detector electronics via optical links and perform energy reconstruction and calibration. Energy values are transmitted to the TDAQi for every bunch crossing. The TDAQi receives data from four CPMs, corresponding to four adjacent phi regions. Additionally, the CPMs buffer the cell energies and transmit data to FELIX in the case of a positive trigger decision. The CPMs are also responsible

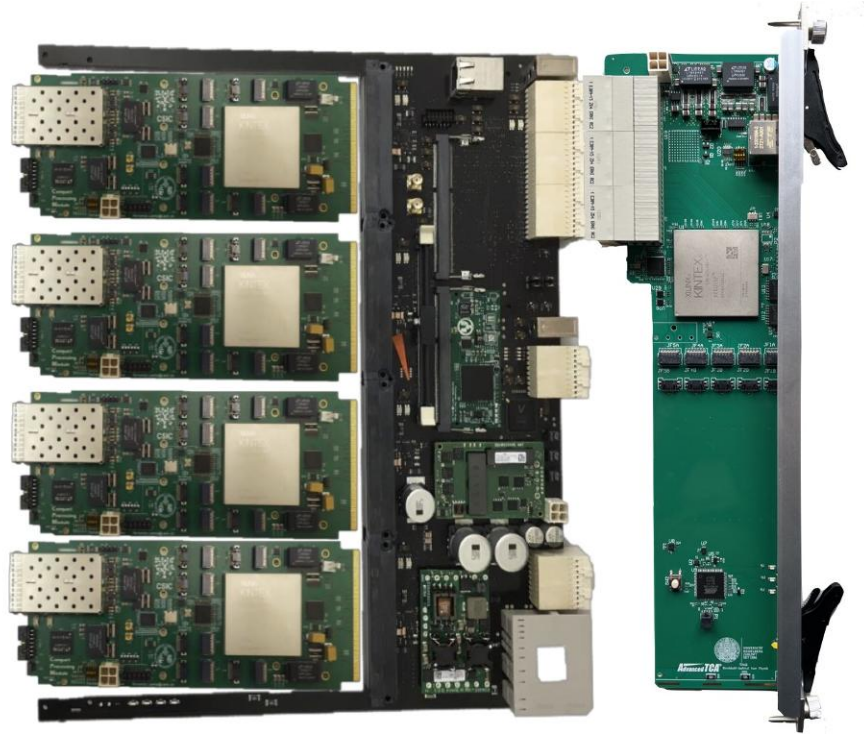


Figure 4.1: The TilePPr module. Four CPMs, which can be seen on the left, connect to the ACBB. The TDAQi, the module on the right, is connected to the carrier board.

for the distribution of clock and configuration signals to the on-detector electronics. For data processing and transmission, the module features an AMD Kintex UltraScale+ Field-Programmable Gate Array (FPGA) [33]. An image of a CPM is presented in Figure 4.2.



Figure 4.2: The Compact Processing Module. Taken from [32].

4.1.2 The ATCA Carrier Base Board

The ACBB is a full size ATCA compliant carrier board. The ACBB manages the communication between the CPMs and the TDAQi, delivers power to the modules, and transmits

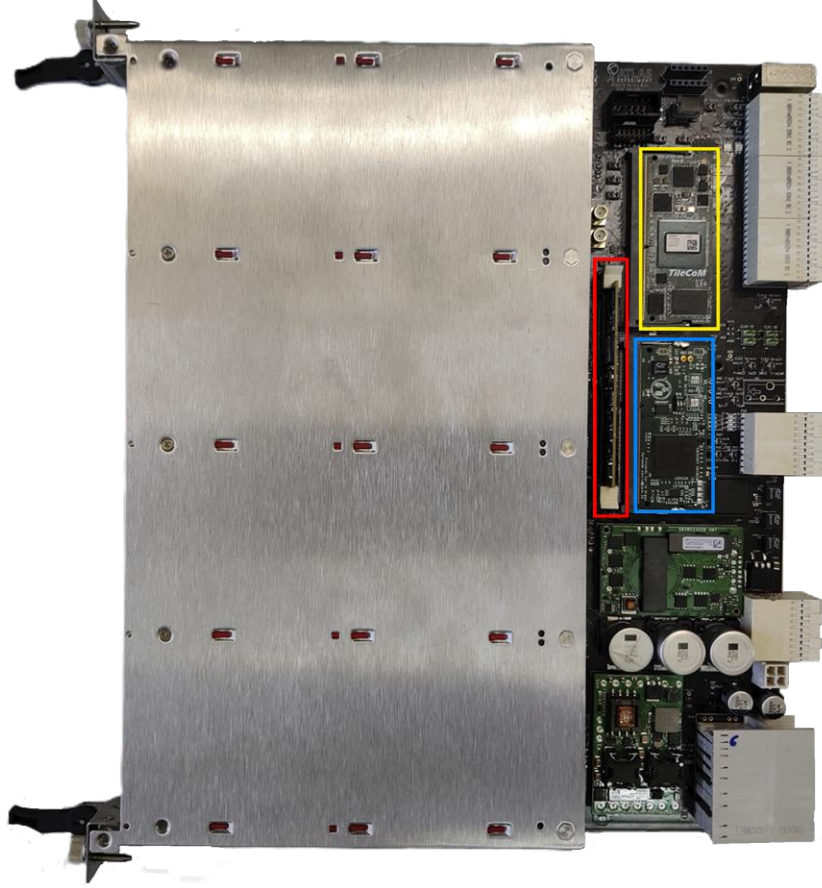


Figure 4.3: The Tile ATCA Carrier Base Board featuring three mezzanine cards, the TileCoM (yellow), the GbE Switch (blue) and the IPMC (red). Adapted from [31].

monitoring data to the Shelf Manager, the unit that monitors the state of all modules in one shelf.

The ACBB features three mezzanine boards, each of which implements different functions [31]. The CERN Intelligent Platform Management Controller (IPMC) [34] is a controller module for ATCA cards. The functions of the IPMC are defined by the ATCA standard and include, for example, monitoring of sensor data and ensuring that the board is in a safe operating state. The Tile Computer-on-Module (TileCoM) establishes communication with the ATLAS Detector Control System and provides an interface with the ATLAS TDAQ system for configuration of on- and off-detector electronics. This module also enables remote programming of the FPGAs. The third mezzanine is a custom Gigabit Ethernet switch (GbE switch) board. It connects the TilePPr to the ATLAS technical and control network. The use of separate mezzanines facilitates future upgrades. In the image in Figure 4.3, the ACBB is displayed and the three mezzanine cards are highlighted.

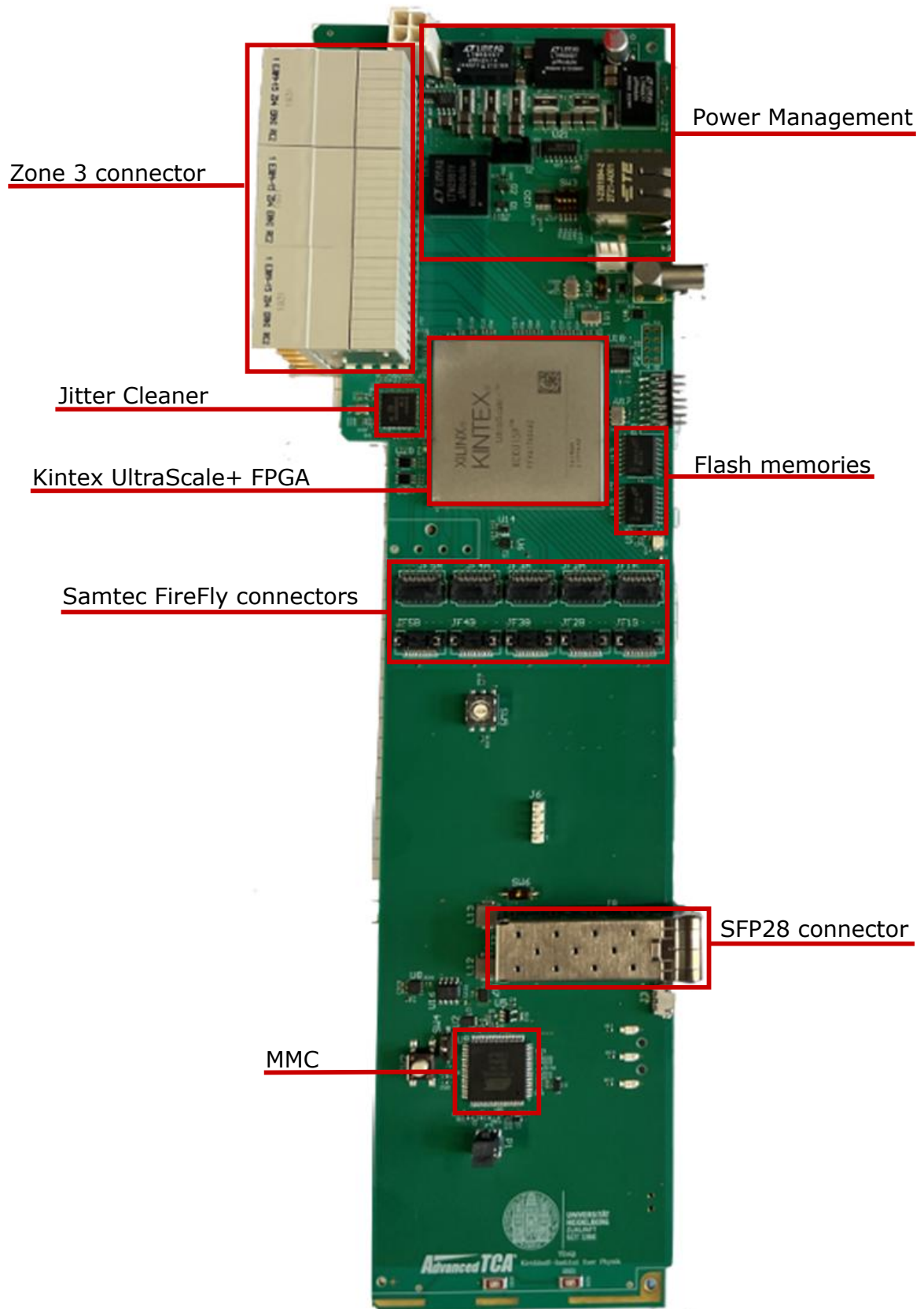


Figure 4.4: The TDAQi without heatsinks, FireFly modules and faceplate. Important components are labeled. Adapted from [35].

4.2 The Trigger and Data Acquisition Interface

The final component of the TilePPr is the TDAQi module [35]. The TDAQi provides inputs to the Level-0 trigger systems for every bunch crossing. To build trigger primitives according to each system's specifications, cell energy values are combined and high-energy cells are identified. For the signal processing and data transmission, a latency budget of 250 ns has been allocated to the TDAQi¹.

The Level-0 trigger reaches a trigger decision within $10\ \mu\text{s}$. Energy values and trigger primitives are stored in pipeline memories on the TDAQi for up to $12.8\ \mu\text{s}$. If the L0A is received, the data for the corresponding event is extracted and transmitted to FELIX. Data is sent to the Level-0 systems and to FELIX via high-speed optical links.

An image of the TDAQi can be seen in Figure 4.4. The main components of the module are labeled in the figure.

4.2.1 Physical Description

The TDAQi [35] is an ATCA Rear Transition Module with a Printed Circuit Board (PCB) measuring $322.25\ \text{mm} \times 70\ \text{mm}$. The module is equipped with a faceplate, although it is not shown in Figure 4.4. The TDAQi features a connector in Zone 3, along with guide pins in Zone 2, the middle section of the board, and above the connector to facilitate alignment.

The data processing algorithms are implemented on the FPGA of the module. Like the CPMs, the TDAQi features an AMD Kintex UltraScale+ FPGA [33, 36]. In addition to generic logic fabric, the device contains specialized blocks optimized for specific functions. These include, for example, Digital Signal Processing (DSP) blocks, I/O blocks, and memory elements. The Kintex UltraScale+ FPGA also contains a large number of high-speed transceivers.

The Module Management Controller (MMC) implements low-level control of the board, such as managing power-up and power-down sequences. In addition, it can initiate resets of the FPGA and control the main voltage output. The MMC is also responsible for monitoring the health of the board and transmitting sensor data to the IPMC.

¹The TDAQi latency budget is given in Table 8.1 in [22].

To generate various clock signals, the TDAQi is equipped with three crystal oscillators and a jitter cleaner unit. The clock signals provided to the FPGA include the 40.08 MHz bunch-crossing clock, which is distributed by the FELIX system, as well as both a 240.48 MHz signal phase-aligned to, and a 280.56 MHz signal phase-locked to the 40.08 MHz reference.

The TDAQi features two flash memories, which can host multiple firmware images to configure the FPGA. When the module is switched on, a minimal firmware image is loaded into the FPGA to establish basic communication functions.

The Zone 3 connector provides high-speed electrical links between the TDAQi and the ACBB. Data from the CPMs is routed through the carrier board and transmitted to the TDAQi via this connection. The Gigabit Ethernet connectivity is also provided through the Zone 3 connector or can be established using the SFP28 transceiver. Ethernet connectivity is necessary to access the module via the IPbus protocol, which will be discussed in Chapter 5.2.3.

The TDAQi is connected to the various Level-0 systems and to FELIX via optical links. In Table 4.1, the number of links and the link speeds to each system are summarized.

System		Input/Output	Number of Links	Link Speed
L0Calo	jFex	Output	12	11.2 Gbps
	eFex	Output	12	11.2 Gbps
	gFex	Output	1 + 1 spare	11.2 Gbps
L0Muon	BSL	Output	4	9.6 Gbps
	ESL	Output	2	9.6 Gbps
L0Global		Output	8	11.2 Gbps
FELIX		Input	1	9.6 Gbps
		Output	1	9.6 Gbps

Table 4.1: Number of optical links and transmission speeds to the different systems.

The TDAQi is powered through the Zone 3 Connector. The ACBB provides two voltages, 3.3 V and 12 V. To generate the required voltages and to maintain power stability, the board is equipped with a number of power management units and DC-DC converters. The FPGA, in particular, requires very stable voltages.

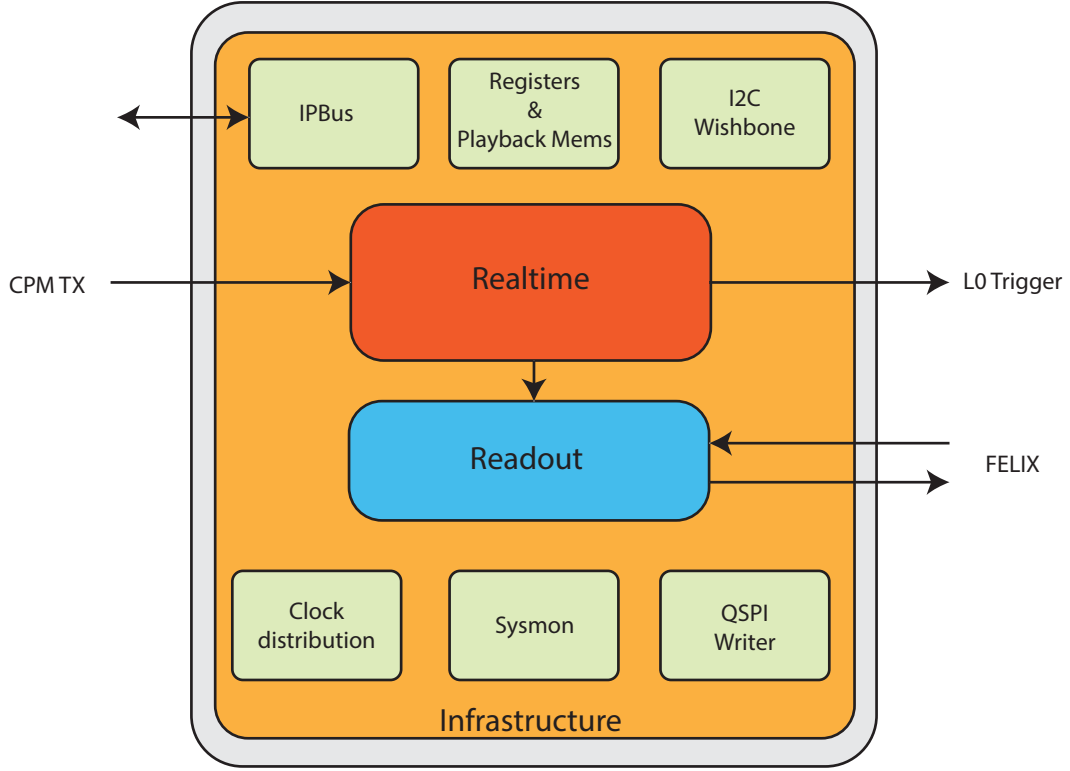


Figure 4.5: Schematic of the top level entity of the TDAQi firmware. Taken from [35].

For the optical transmission to the Level-0 trigger systems and to FELIX, the TDAQi features four 12-channel transmitters and one bidirectional 4-channel transceiver. In Figure 4.4, the connectors for the FireFly modules are indicated. They are mounted close to the FPGA to minimize the length of the high-speed PCB traces.

The FPGA is cooled using a slim heatsink and low-profile fan. Heatsinks are mounted on the FireFly modules as well. For better visibility, the heat management components are missing in the picture in Figure 4.4.

4.2.2 Firmware

The firmware of the TDAQi can be divided into two main parts, the Realtime data path and the Readout data path. In addition to the designated Realtime and Readout libraries, the design includes an Infrastructure library. It contains firmware modules that implement essential functions of the FPGA, such as system monitoring, clock distribution and the communication via IPbus. A schematic view of the top level entity of the firmware is shown in Figure 4.5.

The Realtime data path contains the functionalities related to the 40 MHz trigger path.

Here, incoming cell energies are decoded and trigger primitives are built for the different Level-0 trigger systems. Additionally, the encoding, packaging and transmission of data to the trigger systems is implemented. Intermediate results, including cell energies and trigger primitives, are transmitted to the Readout path for every bunch crossing.

In the Readout data path, the interface with FELIX is implemented. The event data from the Realtime path is stored in pipeline memories until the Level-0 trigger issues an accept decision, after which the corresponding data is extracted from the pipelines and transmitted to FELIX. Furthermore, the TTC signals, which are distributed by FELIX, are received and decoded within the Readout path.

The TTC information includes the following signals:

- **LHC clock:** The 40.08 MHz clock that is synchronous to the bunch-crossing clock of the LHC.
- **Bunch-Crossing Identifier (BCID):** A number between 0 and 3563 associated with a specific bunch crossing. After a full orbit, the number wraps around to 0.
- **Level-0 trigger Accept (L0A):** The signal given by the Level-0 trigger to initiate the readout of the subdetectors and the transmission of data to the HLT.
- **Level-0 Identifier (L0ID):** A unique identifier assigned to each event that was accepted by the Level-0 trigger.

To facilitate tests of the front-end systems of the different subdetectors, the FELIX firmware implements an emulator that simulates the trigger and clock signals delivered by the full TTC system [37].

5 | The Realtime Data Path

In the Realtime path of the TDAQi firmware, incoming cell energies from the CPMs are processed by the corresponding firmware blocks into trigger primitives, which are transmitted to the Level-0 trigger systems. This is part of the real-time trigger path following the 40 MHz LHC clock. Copies of the intermediate results from the Realtime path are routed to the Readout path, where they are buffered and can be transmitted to the FELIX system.

This chapter begins with a general overview of the Realtime path, followed by a detailed presentation of the Level-0 Muon data path. The development and implementation of this part of the firmware is the focus of this work, but the data processing and transmission logic is similar to that employed in the L0Calo and Global data paths.

5.1 General overview

A simplified block diagram of the Realtime entity in the firmware is given in Figure 5.1. The data flow through the high-speed links is marked with red arrows. The numbers of links to the respective Level-0 trigger systems are noted in the schematic.

The TDAQi receives input signals from four CPMs, with each module transmitting data through five electrical links. Initially, incoming energy values are aligned to the LHC clock. Subsequently, alignment between the signals from different CPMs is established by cross-referencing the BCID in the data frames. The two-stage alignment procedure ensures synchronization across all links.

For development purposes, an internal emulator for CPM data was implemented that generates different input data patterns. The data flow is controlled by a multiplexer, which can switch between external inputs and emulated data for all four CPMs independently. Both the type of data pattern and which CPMs should be emulated can be configured with a Virtual Input/Output (VIO) core¹ core.

¹An IP core that can be used to probe and modify signals during runtime.

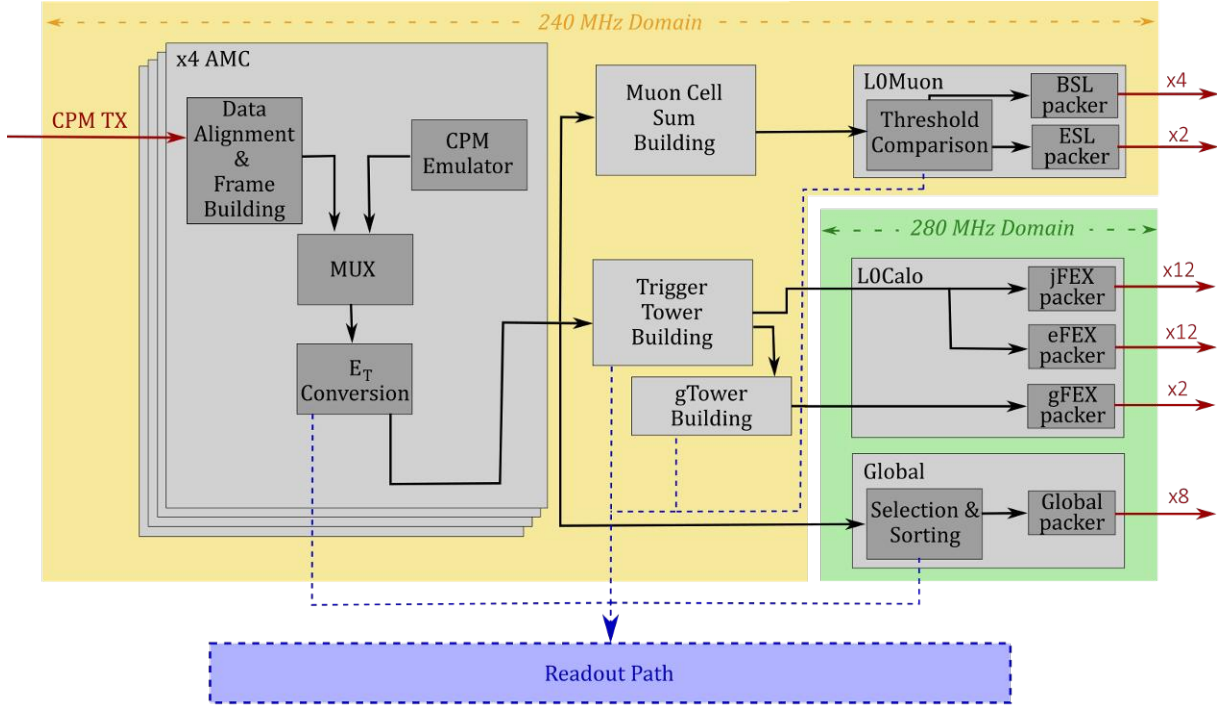


Figure 5.1: Block diagram of the Realtime entity.

The cell energies, whether real or emulated, are converted to transverse energies by multiplication with a sine factor.

Following this conversion, the energy values are used to generate trigger primitives for the different Level-0 systems. The data that is transmitted to the Level-0 triggers is packaged into frames consisting of multiple 32-bit words. The data frames contain some additional information, such as the BCID corresponding to the data and control characters for alignment. The FPGA of the TDAQi features Gigabit transceivers, which are utilized for the transmission.

5.1.1 Trigger Primitives

The trigger primitives generated by the TDAQi firmware are different for each of the Level-0 trigger systems, which are described in Chapter 3.3.1.

For the L0Calo trigger, calorimeter cells are grouped together radially into so-called trigger towers, which correspond to an area of $\eta \times \phi = 0.1 \times 0.1$. For gFex, the trigger towers are further combined into gTowers with a coarser granularity of $\eta \times \phi = 0.2 \times 0.2$. In the case of the Global trigger, cells that exceed an energy threshold of $|2\sigma|$ are collected. In addition, cells with energies higher than $|4\sigma|$ are identified. The cells are sent to the

Global trigger sorted by descending energy. A 23-bit mask identifying which cells exceed $|2\sigma|$ and 15-bit mask for $|4\sigma|$ are transmitted. Finally, 2-bit energy flags are generated by means of a threshold comparison for the L0Muon trigger.

To compute the trigger towers, gTowers and cell sums for the muon threshold comparison, summation modules are implemented. These modules share a similar architecture that leverages the dedicated DSP blocks of the FPGA, which are specialized to perform arithmetic operations. The remaining processing stages, such as the threshold comparison for L0Muon and cell ordering for Global, are executed in the firmware modules for each specific system.

Copies of the trigger primitives are routed to the Readout path of the firmware, where they are buffered. This includes the decoded cell energy values from the CPMs, the trigger tower and gTower values, the muon energy flags, and the bit masks for the Global trigger.

5.1.2 Clock domains

In a firmware design, all modules that are driven by the same clock are referred to as a clock domain. In Figure 5.1 and in subsequent firmware schematics, different clock domains are signified by the background color.

The decoding and processing of the CPM data, the summation of trigger towers, gTowers and muon sums as well as the L0Muon path are all part of the 240.48 MHz clock domain. Conversely, the L0Calo and Global firmware modules operate within the 280.56 MHz clock domain.

The clock speeds correspond to the data rates of the high-speed links to each system. To achieve a transmission rate of 9.6 Gbps, six 32-bit words² need to be sent out per cycle of the 40 MHz LHC clock, requiring a clock speed of 240 MHz. Similarly, seven words in that same time frame are needed for a transmission rate of 11.2 Gbps and correspond to a clock speed of 280 MHz.

The links to Global and L0Calo operate at 11.2 Gbps, while the data routed to the L0Muon system is transmitted at 9.6 Gbps. The incoming links from the CPMs also run at 9.6 Gbps. The number of links and transmission speeds for each trigger system are summarized in

²With 8b/10b encoding, each 32 bit words expands to 40 bits. The data rate is therefore $6 \times 40 \text{ bit} \times 240 \text{ MHz} = 9.6 \text{ Gbps}$.

Table 4.1.

5.2 The L0Muon Data Path

To construct the trigger primitives for the L0Muon trigger, sums of calorimeter cell values are computed which are then evaluated against two thresholds. The summation strategy accounts for cases where the muon energy is deposited across multiple calorimeter cells. Each cell sum is compared against a high and a low threshold, one to identify muons in proximity to a jet and one for isolated muons. In this way, 2-bit energy flags are generated for every sum. If a threshold is met, the corresponding bit is set to 1. The threshold values can be configured using two registers which can be written to using IPBus.

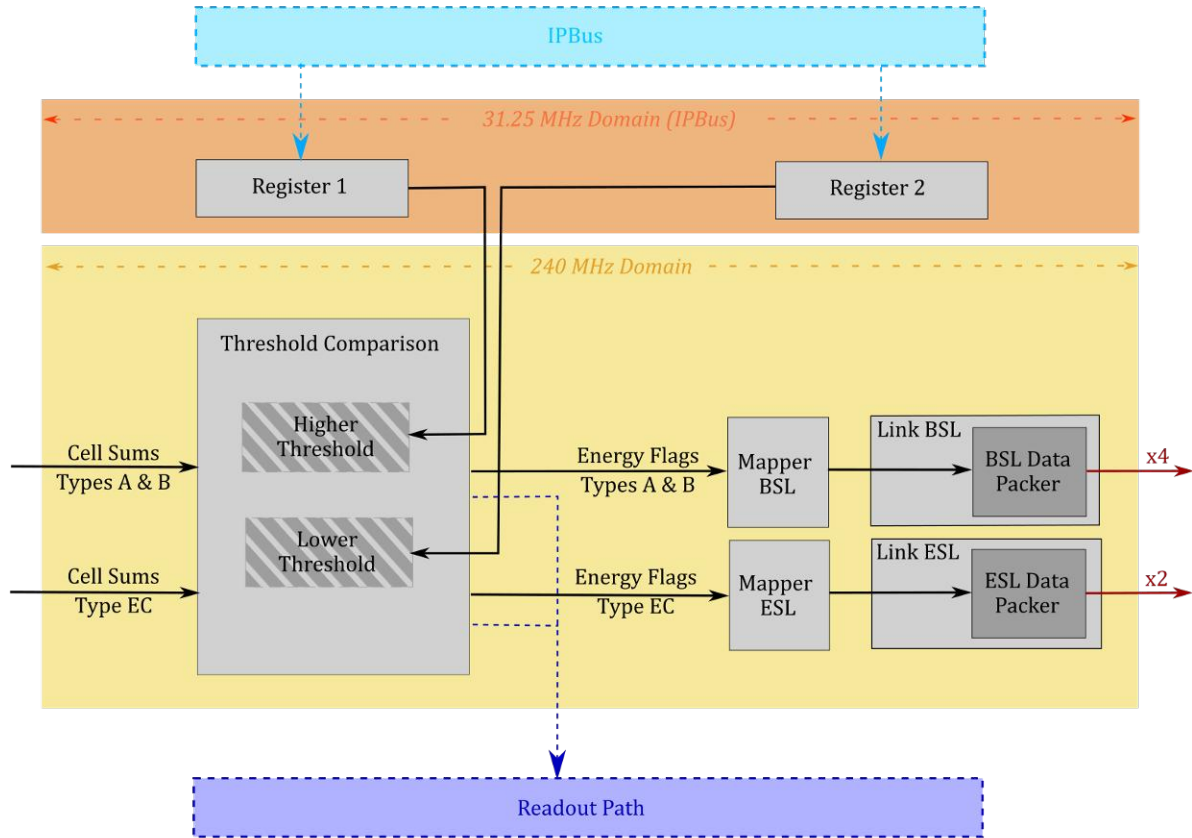


Figure 5.2: Schematic view of the L0Muon entity.

The computed energy flags are packaged into data frames and transmitted to the L0Muon system via six high-speed links. Four of these links connect the TDAQi to the BSL, while the remaining two route data to the ESL.

The threshold comparison as well as the data packaging and transmission through the high-speed transceivers are all implemented within the L0Muon entity of the firmware. A schematic view of this entity is shown in Figure 5.2. Notably, this entity does not contain the summation of cells.

5.2.1 Cell Summation

Prior to the threshold comparison, cells of the calorimeter are combined into predefined sums. In some cases, single cells are used, particularly in the outermost layers of the calorimeter. Otherwise, adjacent cells are summed up to form energy estimates for the comparison.

The complete set of predefined sums is given in Table 5.1. The names of the calorimeter cells can be compared to the calorimeter segmentation illustrated in Figure 3.3. There are three "Types" of sums, with Types A and B consisting mainly of cells from the central barrel and Type EC of cells from the extended barrel. Accordingly, energy flags for Types A and B are transmitted to the BSL, whereas the Type EC flags are sent to the ESL.

Future validation studies should investigate whether these specific sums provide the optimal information to the L0Muon trigger. Any adjustments to the defined sums can be implemented quickly and without major structural change.

For the summation procedure, cell values are ordered into arrays such that neighboring cells form the defined sums. For the BSL sums (Types A and B) pairs of adjacent cells are summed up, whereas for the ESL sums (Type EC) triplets of neighboring values are combined. To unify the declaration of the DSP blocks, the arrays are padded with zeros wherever less than two (or three) cell values need to be summed up. A schematic view of the summation module for the muon cell sums is pictured in Figure 5.3.

	Type		
	Type A	Type B	Type EC
1	D5+D4	BC6+BC5	D6
2	D4	BC5+BC4	D6+D5
3	D4+BC8	BC4+BC3	D5
4	BC8	BC3+BC2	B15+B14
5	BC8+D3	BC2+BC1	B14+B13+B12
6	D3	A10+A9	B13+B12+B11
7	D3+D2	A9+A8	A14+A13+A12
8	D2	A8+A7	A13+A12
9	D2+D1	A7+A6	
10	D1	A6+A5	
11	D1+D0	A5+A4	
12	D0	A4+A3	
13	B9	A3+A2	
14	BC7	A2+A1	
15	BC7+BC6	D5	

Table 5.1: The defined cell sums for the Barrel SL (Type A and Type B) and Endcap SL (Type EC). With 2-bit energy flags, 30 bits are needed to represent the results for Types A and B each and 16 bits for Type EC.

The summation is implemented using the DSP48E2 slices [38] integrated into the UltraScale architecture. Figure 5.4 shows a simplified block diagram of one of these slices. Each DSP48E2 unit has four input ports (A, B, C and D) with different maximum bit widths and one output port (P). In this application, no multiplication is performed, so port B is disabled. By design, the DSP processes two's-complement inputs and performs signed arithmetic.

In this implementation, each DSP slice processes three 16-bit inputs. For the barrel sector sums, one input port is tied to zero. The 16-bit width aligns with the bit width of the energy values transmitted to the TDAQi by the CPMs. The DSP output has a width of 18 bits, ensuring that no arithmetic overflow can occur. To ensure the correct signedness of the input vales, they are extended by one bit that is set to 0. The output width is also

extended by one bit, which is truncated.

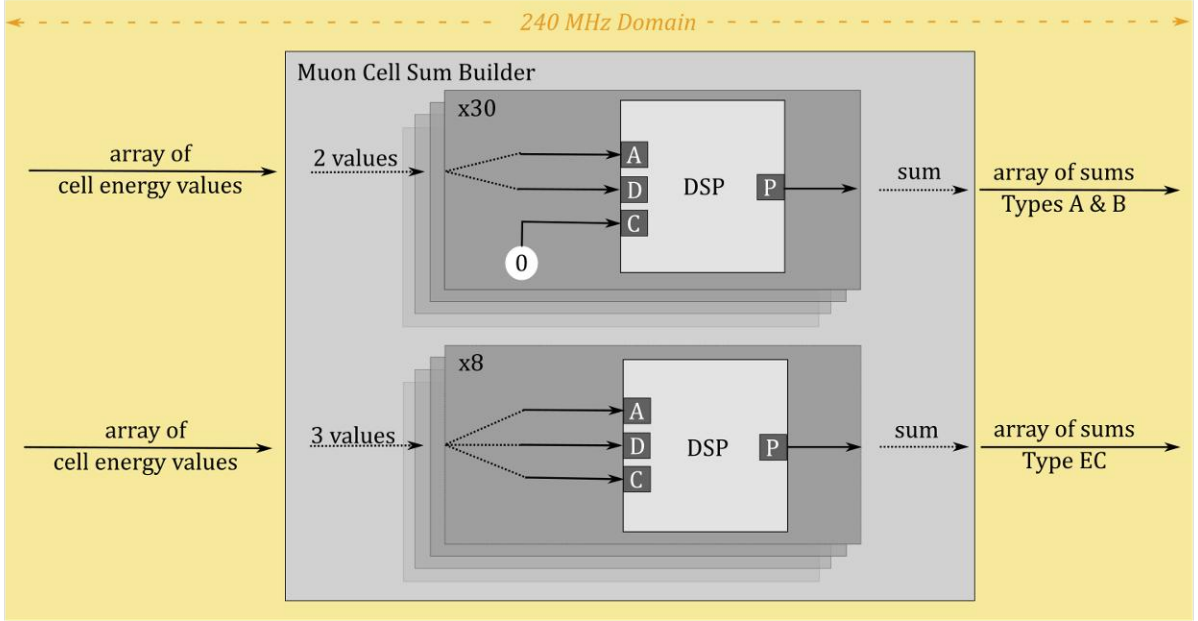


Figure 5.3: Schematic view of the summation module.

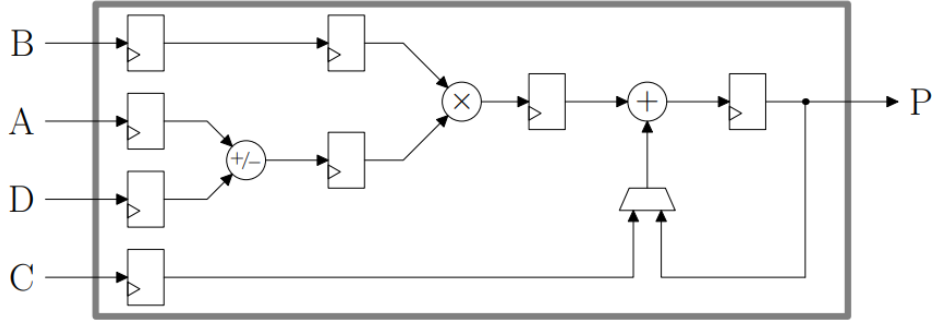


Figure 5.4: Block diagram of a DSP slice. Taken from [39].

5.2.2 Threshold Comparison

The cell sums are compared against two threshold values. If an energy value surpasses a threshold then the corresponding bit is set to 1. Since there are two threshold comparisons, the energy flag for each cell sum is a 2-bit value. The first bit always corresponds to the low threshold, the second to the high threshold.

If the sum value exceeds both thresholds, the flag is set to *11*. If the lower threshold is met but not the higher, the flag is set to *10*. In the case where neither threshold is met the flag is set to *00*.

The firmware logic does not verify that the value for the high threshold is actually larger. This will be checked upon configuration of the registers. Without this verification, the threshold comparison can yield invalid energy flags, as the ordering of the bits will be flipped.

Thresholds are configured via two dedicated registers, each of which can hold 152 entries. This means that for each of the 38×4 cell sums, two individual thresholds can be set. While detector symmetry suggests that the thresholds should be the same across all four phi regions, the firmware allows for individual threshold configuration to maintain flexibility.

The threshold values are retrieved from the IPbus registers at the frequency of the IPbus clock, which is 31.25 MHz. The values go through a clock domain crossing before being routed to the firmware entity that implements the threshold comparison logic.

5.2.3 Threshold Configuration

The registers used to configure the threshold values can be configured using IPbus. The IPbus protocol [40] is a protocol for controlling IP-aware hardware using software applications. The Phase-II electronic components largely follow the ATCA or μ TCA standards, replacing the VMEbus standard. The xTCA standards implement industry-standard serial communication technologies such as Gigabit Ethernet. Unlike VMEbus, they do not have a defined hardware access protocol. IPbus was developed at CERN to implement a reliable hardware control link. It has been used successfully in large systems, for example in the CMS experiment since the start of Run 2.

The IPBus suite consists of a repository of firmware modules, the Hardware Access Library *μ HAL*, which implements a C++/Python interface, and the *Control hub*, a software application for mediating access from multiple clients. The registers implemented for the threshold values are part of the IPbus Firmware component library.

A Python script was developed to configure the threshold registers, featuring a Graphical User Interface (GUI), which is shown in Figure 5.5. Address file and target device need to be specified to establish a connection via IPBus. The threshold values can be configured either by applying a uniform value for each threshold or by entering .txt files with exactly 152 entries to configure thresholds individually for each cell sum. The script confirms the

correct input file length. Additionally, the threshold hierarchy is validated. If any high threshold falls below the corresponding value of the low threshold, a warning message is displayed.

Figure 5.5: GUI for L0Muon threshold configuration. Address file and target device can be configured in the upper panel, while threshold values or .txt files can be entered in the lower section.

5.3 Transmission to L0Muon

The Kintex UltraScale+ FPGA integrates a number of high speed transceivers. Data transmission to the L0Muon system is implemented using the GTH³ transceivers [41]. Six links to L0Muon are implemented, each operating at a data transmission rate of 9.6 Gbps.

The data is encoded using an 8b/10b scheme, whereby each 32-bit word of the data frames

³Gigabit Transceiver Type H, these are capable of data rates of up to 16 Gbps.

is mapped to a 40-bit word. This encoding ensures the DC balance of the links, meaning over an extended period of time the cumulative number of transmitted ones and zeros remains approximately the same.

5.3.1 Data Frames

The data is packaged into predefined frames, each comprising six 32-bit words. Each processing cycle requires two data frames for the BSL data and one frame for the ESL. Six links connect the TDAQi to the L0Muon systems, four to the BSL and two to the ESL. Each of the three data frames is duplicated and sent via two links.

Tables 5.2 and 5.3 present the data frames that are sent to the BSL. Each frame contains the trigger information for two out of the four phi sectors. A 1-bit data valid flag (denoted "V" in the tables) can relay detector status information transmitted by the on-detector electronics. The frames contain the serial number of the board sending the data ("TDAQi-ID") alongside the 12-bit BCID. To ensure data integrity, an 8-bit Cyclic Redundancy Check (CRC) is appended to the data frame. "K28.5" is a control symbol in 8b/10b encoding, which is included for data alignment purposes. Unused bit fields are marked in gray in the tables and set to 0 during transmission.

In Table 5.4 the frame structure for the ESL data is displayed. All energy flags corresponding to the endcap sector fit into a single frame, which is transmitted across two links. This frame contains the same metadata and control symbols as the BSL frames.

	word content																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																	TDAQi-ID				BCID											
1		V	Type A (Phi Sector 0)																													
2		V	Type B (Phi Sector 0)																													
3		V	Type A (Phi Sector 1)																													
4		V	Type B (Phi Sector 1)																													
5	CRC-8																									K28.5						

Table 5.2: First Data Frame for Barrel Sector Logic.

	word content																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																	TDAQi-ID				BCID											
1		V	Type A (Phi Sector 2)																													
2		V	Type B (Phi Sector 2)																													
3		V	Type A (Phi Sector 3)																													
4		V	Type B (Phi Sector 3)																													
5	CRC-8																									K28.5						

Table 5.3: Second Data Frame for Barrel Sector Logic.

	word content																																	
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0																	TDAQi-ID				BCID													
1																	V	Type EC (Phi Sector 0)																
2																	V	Type EC (Phi Sector 1)																
3																	V	Type EC (Phi Sector 2)																
4																	V	Type EC (Phi Sector 3)																
5	CRC-8																					K28.5												

Table 5.4: Data Frame for Endcap Sector Logic.

6 | The Readout Data Path

The Readout data path of the TDAQi firmware implements the interface with the FELIX system. The FELIX system routes TTC signals to the front-end electronics of the detectors and collects event fragments from the front-end pipelines when the Level-0 trigger reaches a positive trigger decision. In the Readout path, those TTC signals are recovered, copies of intermediate results from the Realtime path are buffered, and data is transmitted to FELIX if the L0A signal is received.

A general overview of the Readout data path is presented in this chapter. Since a significant part of this work includes the integration of the L0Muon data into the Readout path, a detailed description of each processing stage is given. All data types that are included in the readout data package traverse parallel instances of this processing path.

6.1 General Overview

A simplified block diagram of the Readout entity in the firmware is shown in Figure 6.1.

The results from the Realtime path pass through a clock domain crossing when they enter the Readout entity. These results include the decoded cell energies, trigger towers, gTowers, muon energy flags, and bit masks for the Global trigger.

For each of these data types, a pipeline is implemented. The data pipelines are circular buffers that can store the data for up to $12.8\,\mu\text{s}$, or 512 bunch crossings. This is enough time for the Level-0 trigger to make a decision and for the L0A signal to reach the TDAQi.

The buffers are implemented using the Ultra RAM (URAM) resources of the FPGA. To ensure that the correct data is extracted, the URAM blocks utilize address pointers that are controlled via IPBus registers. For all data types, the address pointers can be configured individually.

Once the L0A signal for an event is received, the corresponding data is extracted from the pipelines and placed into the derandomizer. The derandomizer implements First-In,

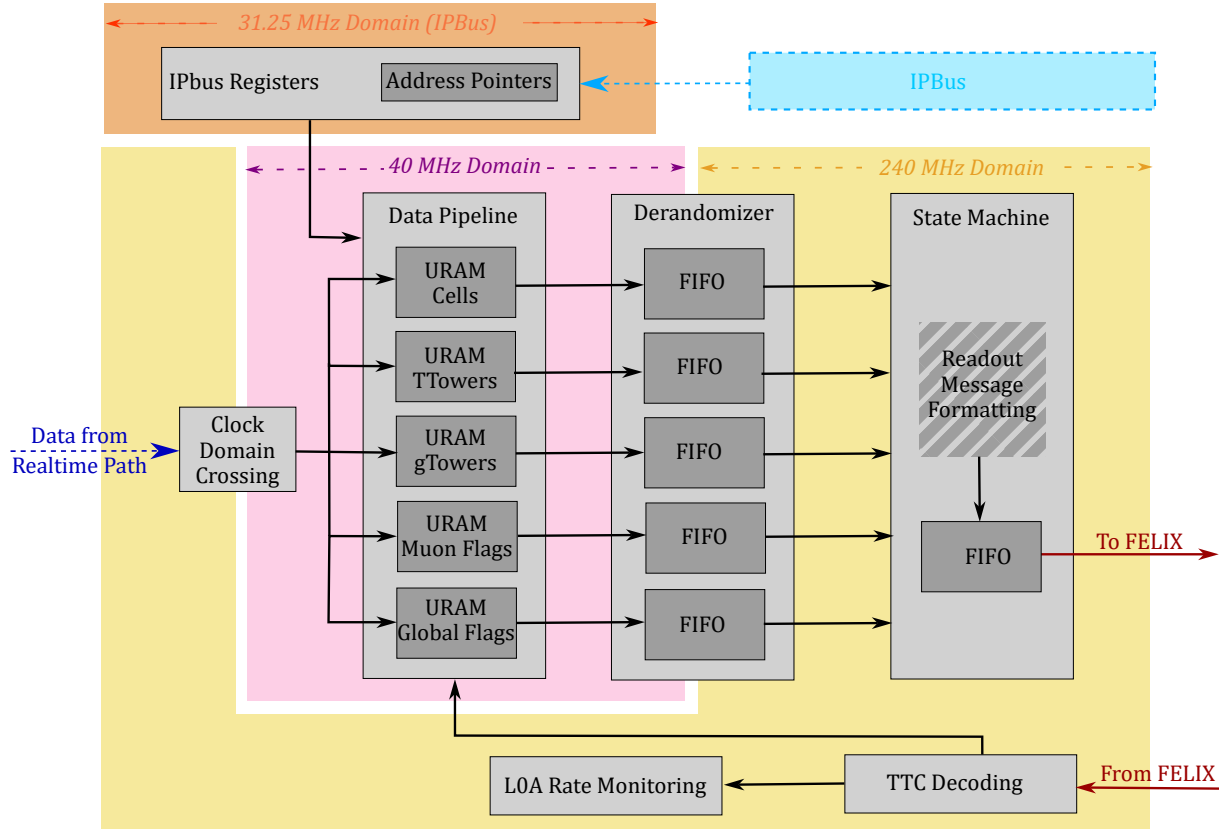


Figure 6.1: Block diagram of the Readout entity.

First-Out (FIFO) buffers for each data type, as well as for the Level-0 Identifier (L0ID) and BCID, which are provided by FELIX. The latter are omitted from the block diagram in Figure 6.1.

A state machine controls the transmission to FELIX. The different data types are sent out one after the other, framed by a header and trailer words that contain metadata for the event. The data is placed into a 64-bit wide FIFO before it is passed along to the transmitter logic. The readout message is transmitted to FELIX in increments of 32-bit words.

The incoming TTC signals are decoded and distributed throughout the TDAQi firmware. Relevant signals in the TTC message are described in Chapter ??.

6.1.1 Clock domains

The data coming from the Realtime path passes through a clock domain crossing from the 240 MHz domain to that of the 40 MHz LHC clock before entering the pipeline entity.

The pipeline needs to be part of the 40 MHz clock domain because the data coming from the Realtime path only changes at the bunch-crossing rate of the LHC. Therefore, the 40 MHz clock is used to avoid writing the same results into the buffers multiple times.

The transmission to FELIX is implemented in the 240 MHz clock domain, matching the word clock speed for the transmission rate of the link, which is 9.6 Gbps. The clock domain crossing back into the 240 MHz domain is implemented in the derandomizer module. The FIFOs are written to with the 40 MHz clock but read out at 240 MHz.

6.2 Data Pipeline

The results from the Realtime path need to be stored until the Level-0 trigger reaches a decision. The ATLAS TDAQ system requires event data to be saved for at least $10\ \mu\text{s}$ to give the Level-0 trigger sufficient processing time. The TDAQi implements buffers that can store data for up to $12.8\ \mu\text{s}$, which is equivalent to 512 bunch crossings.

For the pipeline, the internal memory resources of the FPGA are utilized. The UltraScale+ FPGAs feature memory blocks in the form of Block RAM (BRAM) and URAM [42].

BRAM blocks are more flexible and are more evenly distributed throughout the FPGA, which simplifies routing and logic placement. The two ports of the BRAM blocks can be configured completely independently. URAM blocks are optimized for larger buffers and have a much larger capacity but are not as flexible. For example, URAM blocks cannot be clocked independently on each port. BRAM blocks are utilized in latency-critical applications where lower memory density is sufficient, whereas URAM blocks are used when larger buffers are needed.

In this application, the pipelines need to store considerable amounts of data, therefore the URAM blocks are utilized. The potential delay from routing is not an issue because in the Readout path, latency is not a critical concern.

The URAM is implemented as a dual-ported RAM, with a common clock for both ports. This means that read and write operations can be performed at the same time¹.

The write address and read address are incremented synchronously with the 40 MHz clock.

¹Unless read and write operations target the same address in the same clock cycle. In this configuration, the memory at that address is updated but the output remains at the value from the previous cycle.

The pipelines are circular buffers, meaning once either of the address counters reaches 512, which is the depth of the buffers, it wraps around to 0.

The read address and write address are related as follows:

$$\textit{Read Address} = \textit{Write Address} + \textit{Address Pointer}. \quad (6.1)$$

The address pointer controls the offset between the read and write addresses and can be configured using IPbus. For all URAM blocks, a dedicated register is implemented, so that address pointers can be configured for different data types individually.

6.2.1 Address Pointers

The construction of different trigger primitives requires various amounts of time, as the algorithms vary in complexity. Therefore, different types of data from the same bunch crossing arrive in the Readout path at different cycles of the LHC clock. This is illustrated in Figure 6.2. For example, the gTowers arrive two LHC clock cycles after the trigger towers. This reflects the processing chain, as the gTowers are built from the trigger towers with two additional rounds of summation, i.e., four trigger towers are summed up pairwise and then combined.

To ensure that the data is synchronous, variable address pointers are used. They control the offset between the read and write addresses of the buffers, as referenced in Equation 6.1. The relative offset of all data types that are transmitted to FELIX is corrected by aligning the data to the path with the highest latency, as illustrated in Figure 6.2.

Since firmware behaves deterministically with each process requiring a fixed amount of time, the offset between different data types can be calculated once and the address pointers set accordingly.

Figure A.1 in the appendix shows the signals captured by an Internal Logic Analyzer (ILA) core², where the shift as displayed in Figure 6.2 can be observed. In Chapter 7.2.2, the offset between the cell values and muon flags is measured externally by calculating the mismatch rate with different pointer settings.

²This is an IP core to observe internal signals in an FPGA.

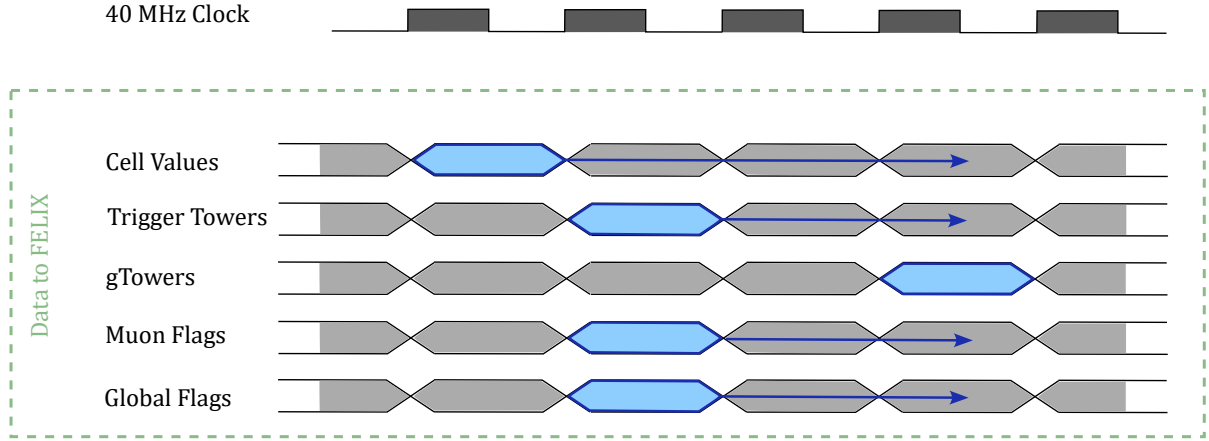


Figure 6.2: Address pointers are adjusted to aligning the data to the path with the highest latency. For each data type, different pointer values can be configured.

In addition to the relative shift, the pointer can also be used to set the exact buffer time, in accordance with the time the Level-0 trigger requires to make a decision and for the L0A to reach the TDAQi. Since the Level-0 trigger is entirely hardware-based, the latency of the L0A is fixed. Currently, this is not relevant, as the Level-0 system is still under development. Since the trigger latency budget of $10\ \mu\text{s}$ would correspond to 400 cycles of the LHC clock, all address pointer values are expected to be around this value in the final configuration.

6.2.2 Derandomizer

Once the L0A signal is received, data at the current readout pointer is extracted and forwarded to the derandomizer, where it is buffered in a set of FIFOs.

A FIFO ("first-in, first-out") is a buffer from which data is read out in the same order that it was written. When another L0A is issued while the transmission to the FELIX system is still ongoing, the data for that event is not lost, but appended in the FIFO and processed afterwards. Dedicated FIFOs are implemented for all data types as well as for the L0ID and BCID.

The FIFOs are written to with the 40 MHz LHC clock and read out at 240 MHz for the transmission to FELIX. This ensures reliable data transfer across the two clock domains.

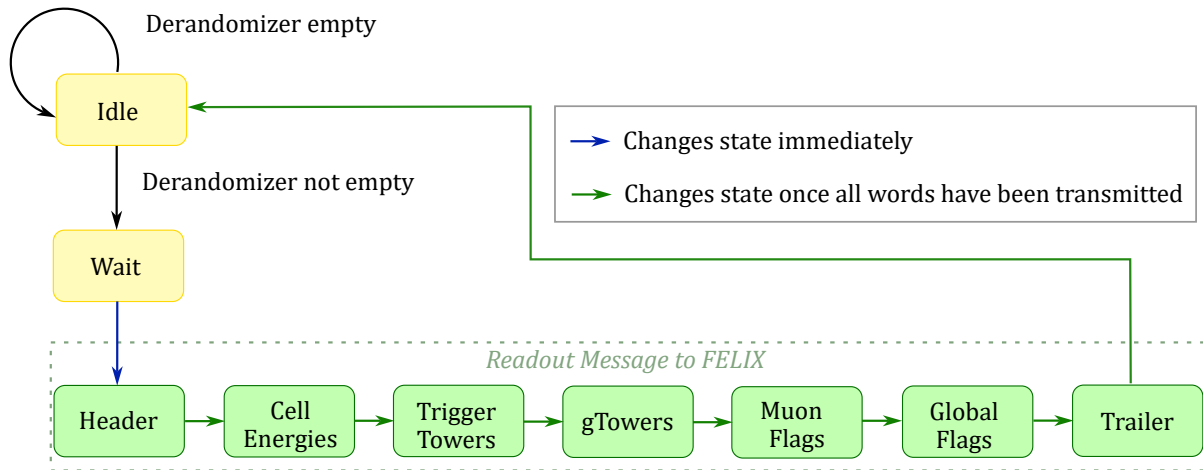


Figure 6.3: Schematic view of the state machine controlling the transmission to FELIX.

6.3 Transmission to FELIX

When the L0A is issued, FELIX receives a message from the TDAQi, which contains all results from the Realtime path, as well as some additional information in the header and trailer. For the transmission to FELIX, the GTH transceivers on the FPGA are utilized. There is one link from the TDAQi to FELIX, which operates at 9.6 Gbps³.

6.3.1 State Machine

The formatting of the data packet sent to the FELIX system is controlled by a state machine.

A state machine is a way of controlling and organizing a series of actions that is often found in FPGA designs. It has a set of defined states, with some conditions to change between them, such as internal counters or specific events, like the press of a button. The state machine can only ever be in one state at a time. In this way, a task can be organized into discrete steps that can be executed in a defined sequence, depending on what events occur.

In this application, the use of a state machine ensures that the data packet to FELIX is assembled reliably and contains all relevant information in a fixed structure. A block diagram of this machine is shown in Figure 6.3.

As long as no L0A is received and therefore no data is transferred from the pipelines to the

³The link to FELIX operates in *Full mode*. The specifications of this protocol are provided in [43].

derandomizer, the state machine stays in its *idle* state. If the FIFOs of the derandomizer are not empty, the machine moves into a *wait* state.

After that, it iterates through the blocks of data that the message to FELIX contains. In each following state, the relevant data is placed into a FIFO in 64-bit increments. Word counters are implemented to determine whether all the data from one block has been transmitted. Once the counter conditions are met, the machine advances to the next state to process the next block of data.

The number of words for each block of data is always the same. If, for example, only one CPM is transmitting data to the TDAQi, the corresponding words from the other CPMs are simply set to zero. The number of 32-bit words in the message is counted during the transmission and inserted into the trailer for debugging and commissioning purposes.

When the state machine reaches the end of the data packet, it moves back to the *idle* state. If the FIFOs of the derandomizer are still not empty, the transmission process starts again.

6.3.2 Readout Message Format

In the current configuration, the data packet sent to the FELIX system by the TDAQi module consists of 190 32-bit words. Figure 6.4 shows the format of the message sent to FELIX. The number of 32-bit words needed for each block of data is given in the schematic.

The message comprises a header and trailer that contain event metadata alongside the payload, which holds the intermediate results of the Realtime path, namely the cell energies and different trigger primitives.

Some notes on the format of each data block are given in Figure 6.4. With the exception of the gTowers, data types are divided into the four phi sectors covered by one TDAQi module. For these data types, the same format is repeated four times, indicated in the schematic with $\times 4$.

The header and trailer of the message contain relevant metadata. The header includes the L0ID as well as the BCID. The trailer contains the word count of the entire message, which is calculated during the transmission.

The format of the message is described here as implemented in the current configuration of

Name	Description of Format	# words
Header	Starts with "00ABCD00" , contains L0ID and BCID	4
Cell energies	5 links with 6 words each ending with "BEEFCAFE" (x4)	120
Trigger Towers	15 Trigger Towers followed by "FFFF" (x4)	32
gTowers	16 gTowers	8
Muon flags (BSL)	15 2-bit threshold flags for Type A and B each (x4)	8
Muon flags (ESL)	8 2-bit threshold flags for Type EC followed by "0000" (x4)	4
Global flags	2-bit flags for all 37 cells (x4)	12
Trailer	Ends with "CAFE0000" , contains the Payload	2

Figure 6.4: Format of the readout message sent to FELIX by the TDAQi. All the signal and filler words explicitly given (in bold letters) are expressed as hexadecimal numbers.

the firmware. It might not contain the same data that will be sent to the FELIX system in the final configuration. For example, transmitting the cell energies might not be necessary as the CPMs already provide them to FELIX⁴. The metadata contained in the header and trailer of the message might be expanded as well, for example by the ID of the board sending the data and error flags asserted for the event. Reconfiguring the contents of the message requires only minor changes to the firmware.

The data packet sent to FELIX provides a way of testing the firmware, as will be shown in Chapter 7.2. In particular, the calculations made in the Realtime path are verified.

⁴However, unlike the TDAQi, the CPMs transmit the cell energy values without converting to transverse energy.

7 | Firmware Validation

Firmware functionality is confirmed through multiple tests. First, the logic that generates the muon energy flags is validated by comparing the cell energies with the muon flags that are transmitted to the FELIX system. The data frames that are transmitted to the L0Muon systems through the optical links are captured using the TREX module, a legacy component of the Tile Calorimeter readout, as an optical receiver. Finally, the processing latency of the L0Muon data path is measured.

In this chapter, the testing environment is described, the methodology for each validation procedure is presented, and the corresponding results are reported.

7.1 Test Setup

Validation testing was performed using the test setup located at the Kirchhoff Institute for Physics in Heidelberg. In this configuration, the pre-production TDAQi modules can be connected to a TilePPr carrier board inside an ATCA crate. The TREX module is utilized to capture the optical output of the TDAQi.

A FELIX PCIe card¹ integrated into a commercial server provides the systems in the test bench with a common clock. The internal emulator of the FELIX firmware is employed to provide the systems with TTC information. Emulator configuration is managed using the FELIX software. The relevant contents of the TTC message are detailed in Chapter 4.2.2. In particular, the L0A signal enables the transmission of data packets from the TDAQi to FELIX. The emulator asserts the L0A signal at regular intervals, with an adjustable repetition rate.

The FELIX card implements optical links to transmit and receive data. Acquired data, such as the readout messages sent by the TDAQi, is made available to the host server. A custom application is used to read out this data and write it into a .txt file. The number of readout messages that are collected in one file can be configured.

¹The setup includes the latest version of this card, FLX-712. [28].

For the tests, the data generator, which is implemented in the TDAQi firmware is used to provide input data. The data generator, which is described in Chapter 5.1, is controlled with a VIO core. Multiple data patterns are available, including both constant and dynamic patterns. Additionally, the generator can be configured to supply data only for some of four phi sectors.

7.1.1 The TREX Module

The Phase-I Upgrade introduced the new L1Calo trigger, described in Chapter 2.2.2, which required digitized optical inputs, as opposed to the analogue inputs that were used by the legacy system. During Run 3, both trigger systems operated in parallel to facilitate commissioning and system validation.

To meet the requirements of the new L1Calo system while preserving compatibility with the legacy components, the TREX module [44] was implemented as a physical extension of the L1Calo PreProcessor. The PreProcessor processed, combined, and transmitted analogue calorimeter signals. The TREX module expanded this functionality by providing the new components with digitized optical inputs, while maintaining communication with the legacy systems.

Data processing on the TREX module is distributed across multiple FPGAs. The module features four Samtec FireFly optical transmitters and one bidirectional transceiver. An optional 12-port optical receiver is integrated on the module but not utilized in standard operation.

As the TREX module was developed in this group in Heidelberg, it is abundantly available and a good candidate to re-use for data reception from the TDAQi. The optical receiver is activated to capture the outgoing data from the TDAQi for the validation. Only the primary FPGA of the TREX module is utilized for these tests, running a dedicated firmware configuration that decodes and aligns the signals from the TDAQi.

7.2 Energy Flag Validation

After the cell summation and threshold comparison, copies of the generated energy flags are placed into the pipeline of the Readout path. If the TDAQi receives the L0A signal, a

data packet that contains the relevant cell energies and trigger inputs is transmitted to FELIX. The exact format of this message is presented in Chapter 6.3.2.

The muon flags and energy values within the same message are compared to validate the generation of the flags. To automate this process, a dedicated validation script, implemented in Python, was developed.

7.2.1 Test Software

The validation script replicates the firmware logic used to generate the muon flags to determine whether the flags and cell energies within each message are consistent. The script extracts the energy values, forms the specified cell sums, and compares them against two thresholds to calculate the corresponding muon flags. The threshold values must be manually configured, as they are not included in the data packet. The computed result is compared to the energy flags actually contained in the message.

The script iterates through all messages in the specified data output file and returns the total number of mismatches. By default, only the error count is returned. Optionally, a summary visualization of the result is generated, a representative example of which is provided in Figure 7.1.

The summary visualization presents a plot of the energy values across successive messages for a single cell to illustrate the input data pattern. The message count in the file, the number of mismatches that were found and the configured thresholds are displayed alongside the plot. In the example in Figure 7.1, uniform thresholds of 50 000 (high) and 10 (low) are applied.

For constant input data patterns, no mismatches between cell energies and muon flags occurred across multiple test iterations. To test dynamic input patterns, the address pointer offset between cell data and muon information needs to be determined.

7.2.2 Address Pointer Calibration

The data in the Readout path is synchronized using variable address pointers before it is transmitted to FELIX, as detailed in Chapter 6.2.1. The address pointers are configured via IPbus registers and can be adjusted for each data path individually. If the pointers are

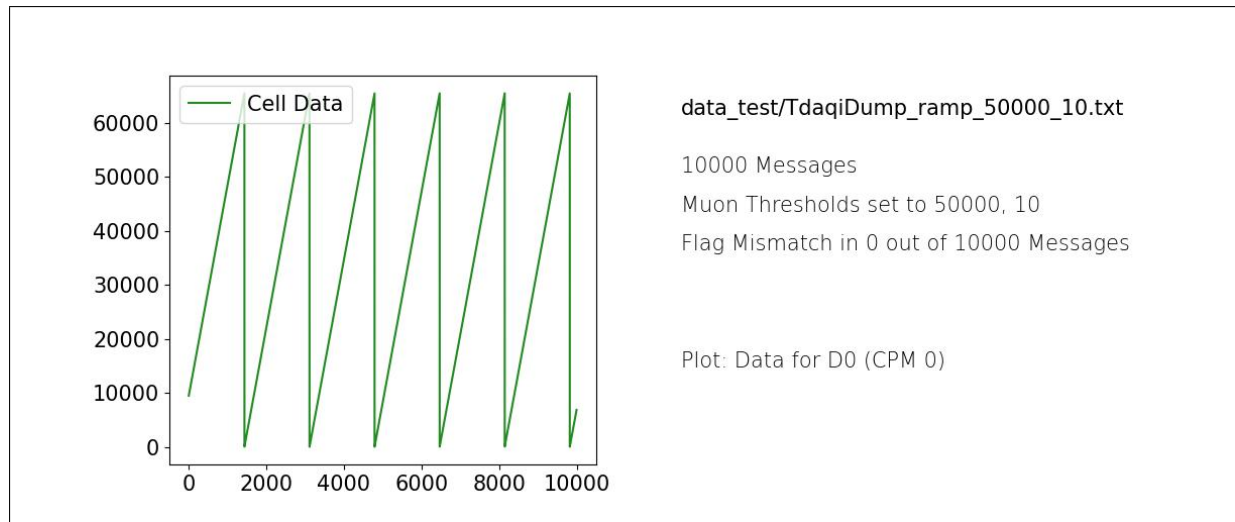


Figure 7.1: Representative summary visualization generated by the validation script. The plot shows the input pattern for one of the cells. The number of messages and mismatches as well as the muon thresholds are annotated within the display.

not adjusted correctly, discrepancies between the muon flags and energy values in the same message might originate from timing mismatches rather than firmware errors. Therefore, the pointer alignment must be verified before tests are carried out.

The calibration is performed by fixing the muon pointer and varying the cell data pointer. An automated script was developed that executes this calibration sequence. The readout messages are captured, the mismatch rate is recorded using the validation script, and the pointer offset is incremented before the process is repeated. Given a sufficiently large message dataset, only one offset configuration with zero discrepancies is expected.

Based on the firmware architecture, it is expected that the muon information arrives only very few cycles of the 40 MHz bunch-crossing clock after the energy information. Consequently, the calibration is confined to cell data pointers within ± 5 increments of the muon pointer. Cell data pointers below the muon pointer fall outside the expected range, but the error rate is calculated to verify baseline consistency.

Figure 7.2 presents two measurements of the error rate as a function of the cell data address pointer value. The error rate was calculated across 20 000 messages per pointer configuration. In both instances, only a single pointer configuration yields zero mismatches, which is a cell pointer offset of +1 relative to the muon pointer. This matches the ILA measurement presented in Figure A.2 in the appendix, where the muon flags are provided one bunch crossing after the energy values.

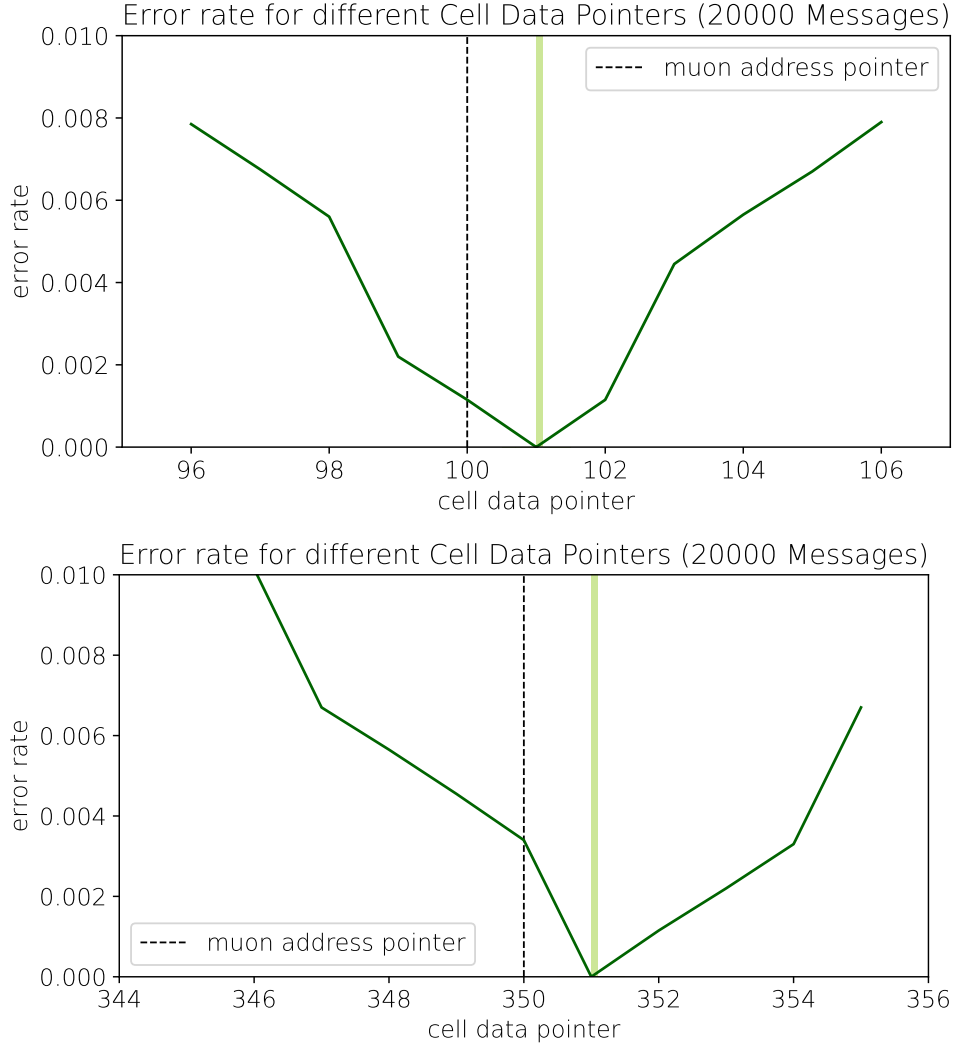


Figure 7.2: Error rate for different cell data pointers. The data pointer for the muon flags is marked with a dashed line. For two different muon pointer settings, the error rate is 0 when the offset is +1.

Overall, the measured error rates remain small because the muon flags only change when a threshold is passed. A mismatch can only be observed if the L0A signal is issued after a threshold crossing but before the muon flags are updated. The duration of this timing window depends on the offset defined by the pointer configuration and decreases as it approaches the optimal alignment. The mismatches become easier to observe when the data pattern and thresholds are configured such that the thresholds are crossed, and therefore muon flags updated, as frequently as possible.

The offset between the flags and energy signals in the firmware was successfully determined through external calibration. The calibration demonstrates that the validation script accurately detects mismatches between cell energies and muon flags. With the correct

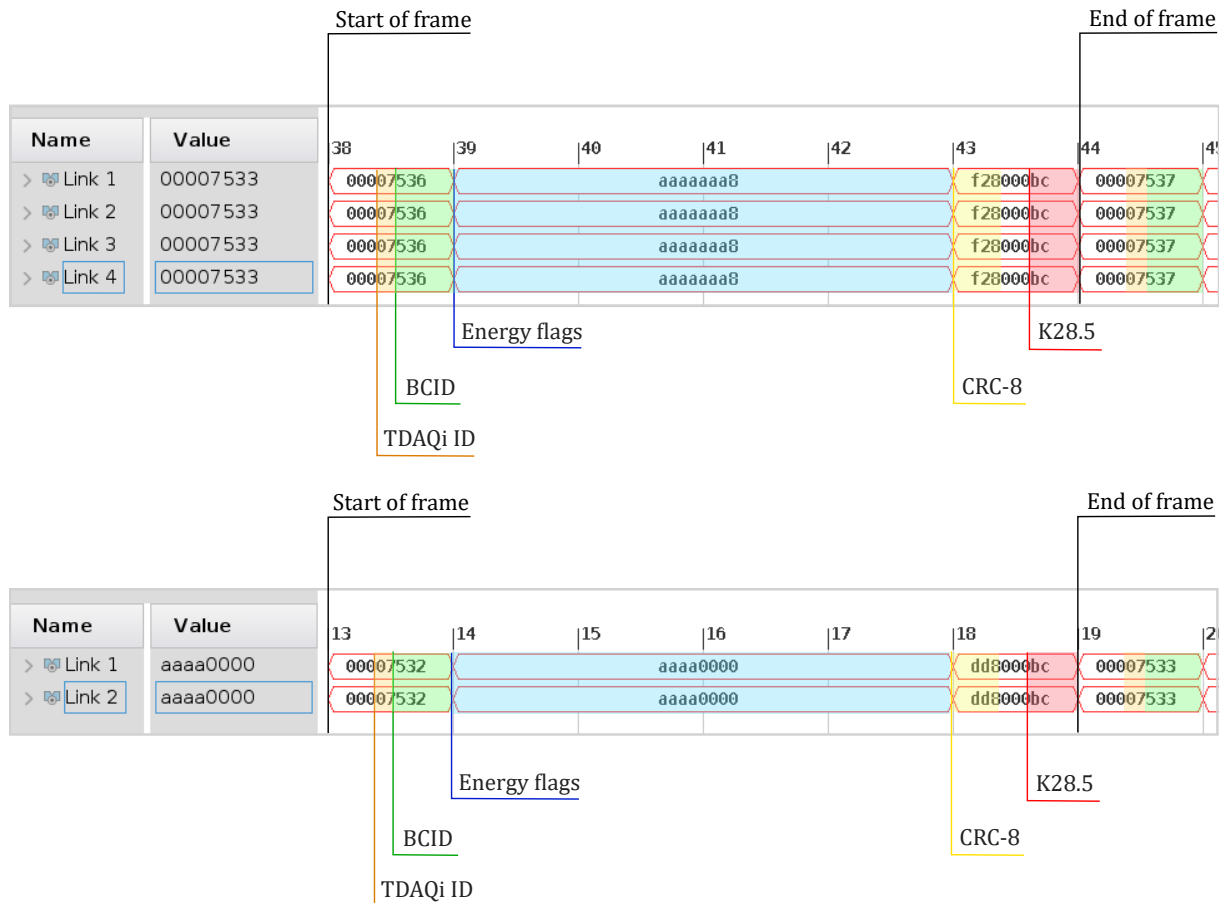


Figure 7.3: Two ILA captures that display the transmitted data frames, with the contents of the frame marked. Signal values are represented in hex format. The upper panel shows the four BSL links, while the lower panel presents the two ESL links.

address pointer offset applied, no mismatches were observed for dynamic input patterns.

7.3 Data Transmission Tests

The energy flags transferred to the L0Muon trigger are packaged into data frames, as was described in Chapter 5.3.1. The correct formatting of the data frames is confirmed by using the TREX module as an optical receiver. A dedicated firmware design for the TREX decodes the data transmitted via the optical links and captures the signals sent by the TDAQi in an ILA core.

The signals captured on the TREX are presented in Figure 7.3. The top panel shows the four links to the BSL, while the two links to the ESL are displayed in the bottom panel. The signals are represented in hexadecimal values and change at a 240 MHz clock rate.

The different contents of the message are marked and can be compared to Tables 5.2, 5.3, and 5.4. The muon flags occupy four words within each data frame. The flags are equal for all links because, in the example, the input data is identical across all cells. The header word includes the hardware ID of the transmitting TDAQi, which is 0x07 in the capture, alongside the BCID. The trailer word contains an 8-bit CRC and the K28.5 comma symbol, which is used for data alignment. The header word of the next frame is visible on the right side of the capture, and the BCID has incremented by 1.

As detailed in Chapter 5.3.1, each data frame is duplicated across two links. Appendix A presents a measurement with input data enabled for only one out of the four phi sectors, demonstrating this duplication.

7.4 Latency Measurement

The latency allocated to the TDAQi is 250 ns. Within this latency budget, CPM data must be decoded, trigger primitives computed, and the resulting signals transmitted. It does not include propagation delays from the transmission to the Level-0 trigger systems through the optical fibers.

For the latency measurement, the input from the internal data generator is set to a ramp pattern. When the ramp crosses zero, a probe signal is asserted on the TDAQi. Correspondingly, when the incoming muon flags turn zero, a probe signal is triggered on the TREX module. The time between the two signals is measured using an oscilloscope. The decoding logic in the TDAQi firmware, which is included in the latency budget, is bypassed by the signals from the internal data generator. However, this is balanced by the signal decoding that is performed on the TREX module.

Figure 7.4 displays the oscilloscope measurement, where statistical results from multiple captures are summarized in the lower panel. The latency was measured to be 205 ns, which is well within the budget of 250 ns.

Additionally, the propagation time through the optical fiber can be subtracted from the measured value. The two fibers between TDAQi and TREX each have a length of 2 m. Given an approximate propagation time for optical fibers of 5 ns/m, roughly 20 ns can be subtracted.

The measured latency represents a preliminary value, as the TDAQi firmware is not yet finalized. Nevertheless, it is demonstrated that the implemented logic satisfies the latency requirements since there will be no major changes to the processing path.

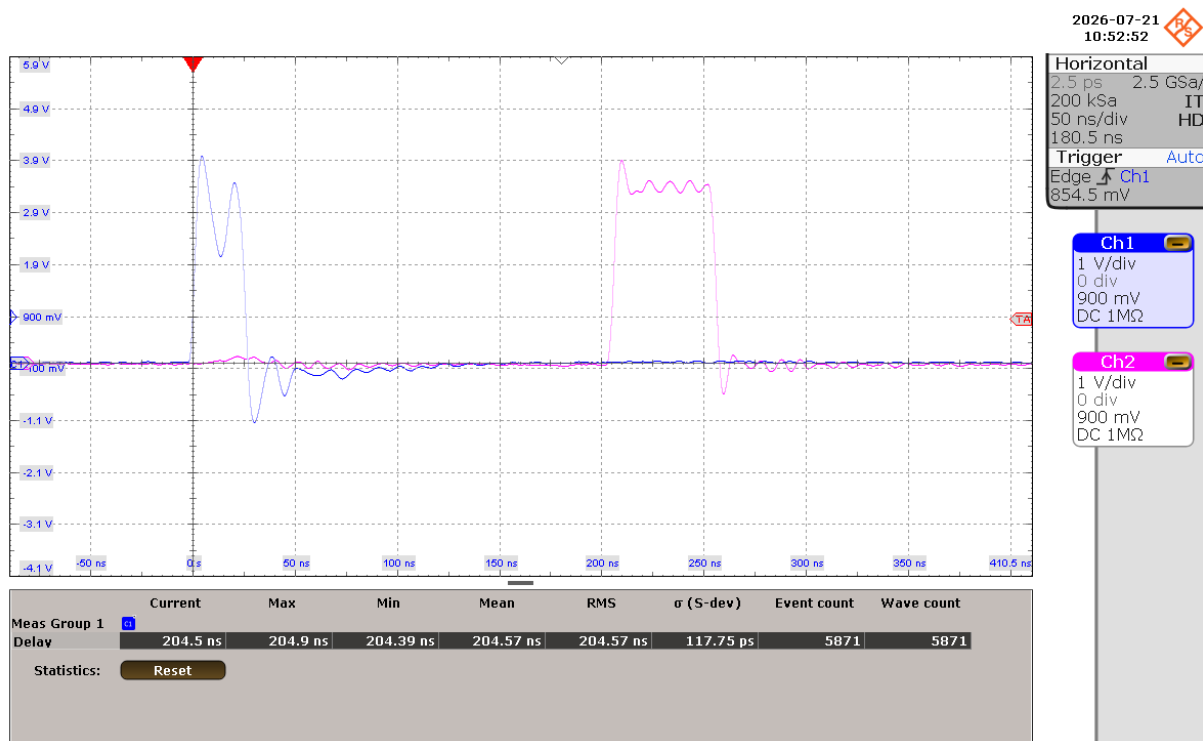


Figure 7.4: Oscilloscope measurement of the latency. The blue signal is generated on the TDAQi when the generated ramp pattern cycles through zero. The pink signal is given on the TRES when incoming muon flags are zero. Results of the measurement are given at the bottom.

8 | Conclusion

To meet the requirements of the High Luminosity Large Hadron Collider (HL-LHC), the ATLAS experiment is undergoing extensive upgrades, which include a redesign of the Tile Calorimeter readout electronics. As part of the revised architecture, the Trigger and Data Acquisition interface (TDAQi) module generates trigger inputs for the Level-0 trigger systems and retains copies of the inputs for potential readout.

The design and implementation of the firmware data path concerning the Level-0 Muon trigger (L0Muon) trigger on the TDAQi module was presented in this thesis. To generate trigger inputs, adjacent cells of the calorimeter are combined, a task realized using the Digital Signal Processing (DSP) resources of the Field-Programmable Gate Array (FPGA) featured on the TDAQi module. Energy flags are generated by means of a threshold comparison. Two registers were integrated to store individual threshold values for all 152 cell sums per hardware module. These can be conveniently configured using the IPbus protocol and a software application for this configuration was developed. The energy flags, alongside metadata about the respective event, are packaged into data frames and transmitted to the L0Muon systems via optical links running at 9.6 Gbps. The muon flags were integrated into the readout data package. To this end, pipeline memories were implemented using the designated memory resources of the FPGA and the state machine controlling the package assembly was modified accordingly.

Firmware functionality was verified through comprehensive testing. A dedicated validation script confirmed correct trigger primitive generation by cross-referencing energy values and muon flags in the readout data package. Data frame assembly was validated by capturing the output through the optical links. Finally, the processing latency of the data path was measured and confirmed to remain well within the latency budget allocated to the TDAQi.

The integration of the L0Muon data path marks an important step towards the completion of the TDAQi module. With the firmware approaching finalization and validation routines established, the project is on schedule for operation at the HL-LHC in 2030.

A | Appendix

Offset between different Data Types in the Readout Path

Figure A.1 presents the signals routed from the Realtime path to the Readout path of the firmware, captured by an ILA core. An internally generated ramp pattern is used as the input signal. As discussed in Chapter 6.2.1, the cell energies and different trigger primitives arrive in different cycles of the LHC bunch-crossing clock. The blue marker indicates when the cell energies drop to zero; the red marker shows the trigger towers and muon flags updating in the next clock cycle; the yellow marker indicates the gTowers changing after three cycles.

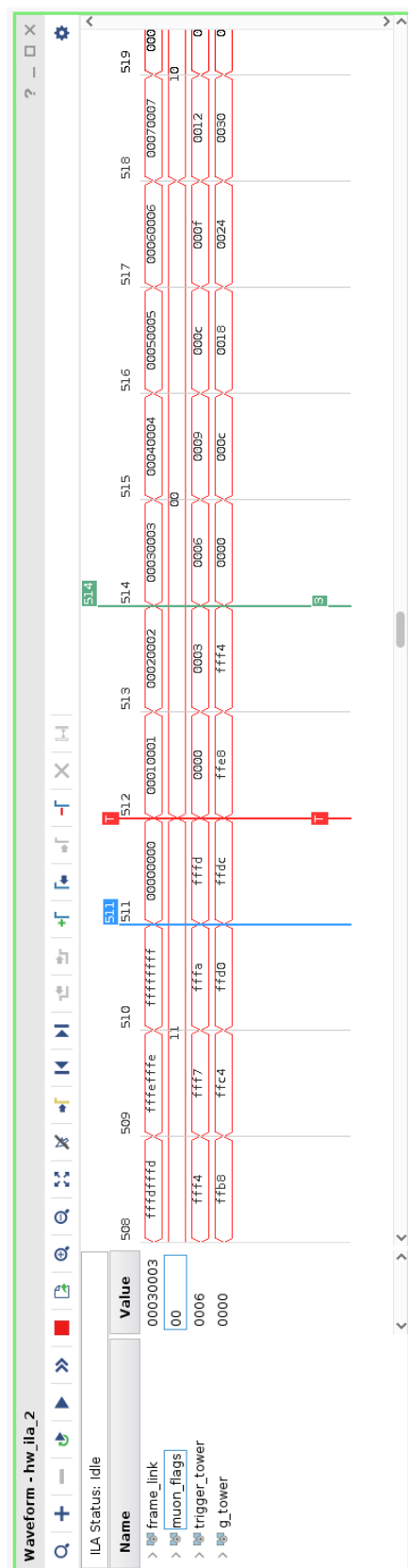


Figure A.1: ILA measurement of the different signals entering the Readout path.

L0Muon Data Frames with three CPMs deactivated

Figure A.2 presents the TDAQ_i optical output captured by an ILA core on the TREX module. This is the same measurement that was described in Chapter 7.3, but the internal data generator is configured to supply values for only one phi region (one CPM), leaving the other inputs at zero. The measurement illustrates the flag placement within each frame, which can be compared to Tables 5.2, 5.3, and 5.4, as well as the link duplication.

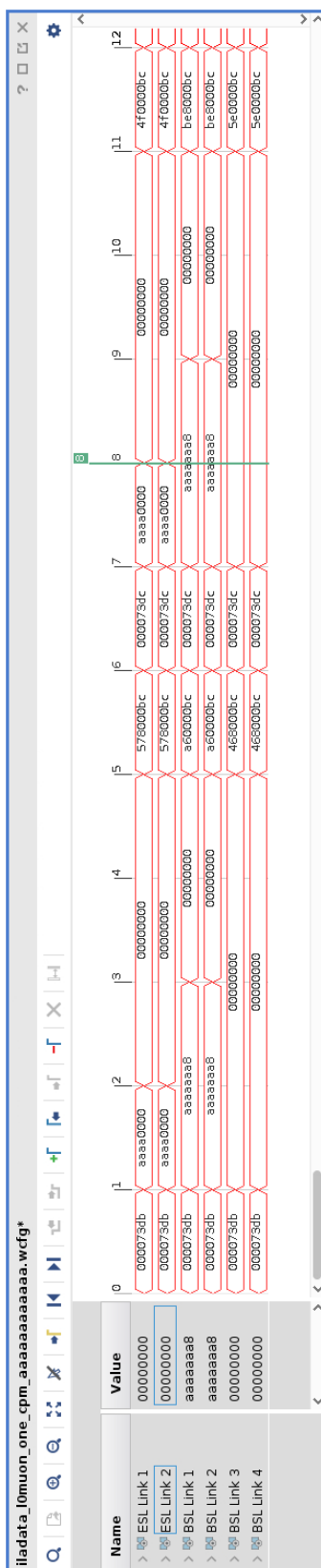


Figure A.2: ILA measurement of the transmitted L0Muon data frames with 3 CPMs deactivated.

Acronyms

ACBB ATCA Carrier Base Board

ADC Analog-to-Digital Converter

ATCA Advanced Telecommunications Computing Architecture

BCID Bunch Crossing Identifier

BSL Barrel Sector Logic

BRAM Block RAM

CPM Compact Processing Module

CRC Cyclic Redundancy Check

CTP Central Trigger Processor

DSP Digital Signal Processing

eFEX electron Feature EXtractor

ESL Endcap Sector Logic

FELIX Front-End Link eXchange

FENICS Front End board for the New Infrastructure with Calibration and signal
Shaping

fFEX forward Feature EXtractor

FIFO First-In, First-Out

FPGA Field-Programmable Gate Array

GbE switch Gigabit Ethernet switch

gFEX global Feature EXtractor

HL-LHC High Luminosity Large Hadron Collider

HLT High-Level Trigger

ID Inner Detector

ILA Internal Logic Analyzer

IPMC Intelligent Platform Management Controller

ITk Inner Tracker

jFEX	jet Feature EXtractor
L0A	Level-0 Trigger Accept
L0Calo	Level-0 Calorimeter trigger
L0ID	Level-0 Identifier
L0Muon	Level-0 Muon trigger
L1Calo	Level-1 Calorimeter trigger
L1Muon	Level-1 Muon trigger
L1Topo	Level-1 Topological trigger
LAr	Liquid Argon
LHC	Large Hadron Collider
LS	Long Shutdown
MDT	Monitored Drift Tube
MMC	Module Management Controller
MS	Muon Spectrometer
NSW	New Small Wheel
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMT	Photomultiplier Tube
RPC	Resistive Plate Chamber
SCT	Semiconductor Tracker
SL	Sector Logic
TDAQ	Trigger and Data Acquisition
TDAQi	Trigger and Data Acquisition interface
TGC	Thin Gap Chamber
TileCoM	Tile Computer-on-Module
TilePPr	Tile PreProcessor
TTC	Timing, Trigger and Control
TREX	Tile Rear Extension
TRT	Transition Radiation Tracker
URAM	Ultra RAM
VIO	Virtual Input/Output

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Acknowledgments

I would like to thank Prof. Hans-Christian Schultz-Coulon for the opportunity to complete my thesis in the ATLAS group in Heidelberg. I enjoyed my work a lot and I appreciate the support I have received throughout my time in the group. I also want to thank Prof. Klaus Reygers for taking the time to read my thesis as the second examiner.

I am grateful to the members of groups F8 and F11 for the positive, supportive work environment and the countless times they helped me with any number of problems. Many thanks to Anke, Isa, Mathias, Tobias and Rainer for proofreading parts of my thesis and providing valuable feedback.

A big thanks to Thomas for his support throughout my thesis, for the many, many questions he answered, and for some encouraging words in the right moments. Thanks to Maximilian, who always found time to help me when I showed up with some new firmware issue or some other technical difficulty that I could not solve on my own.

I want to thank my friends for the walks and coffee breaks that helped me through the more stressful weeks of this work. I am especially grateful to Felix, who shared an office with me and always took the time to chat for a moment.

Finally, I want to thank my grandmother, my brothers, and my parents. Your ongoing encouragement, the interest you show in my work and your unconditional support mean the world to me.

Declaration of AI Use

During the writing of this thesis, I utilized the AI tools provided by the University of Heidelberg (YoKI) for proofreading (grammar, spelling, punctuation) and to help with the translation of the abstract into german.

Erklärung

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