Advanced Analog Building Blocks
Transistor Level Logic

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Standard cells

Digital logic are in fact analog circuits

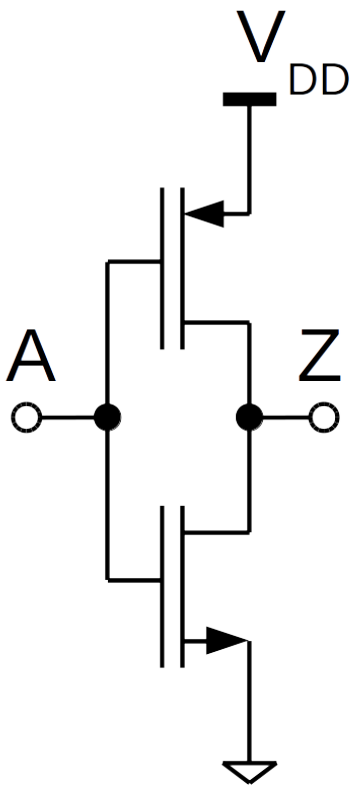
Yes that's true!!

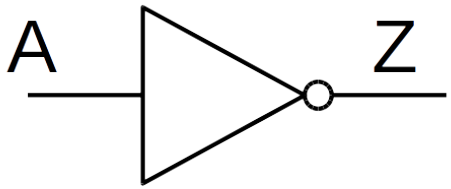
- Set of "basic blocks" grouped in Standard Cells.
- CMOS: Complementary metal-oxide-semiconductor, from complementary structures in logic.
- Standard Cells have several constrains/characteristics;
  - Fixed height and variable width.
  - Fixed position of VDD and GND.
- Set of important characteristics;
  - Delay/speed.
  - Power consumption.
  - Driving power.

- Rising/falling edge:
  - **Designed to have same rising and falling time at output!!**
- Driving power:
  - Is measured as integer values of how much simple inverters the cell can drive.
  - Naming convention: INV1, INV2,... AND1,AND2,...

Combinational logic: Inverter

Simpler cell is an inverter (remember amplifiers?).

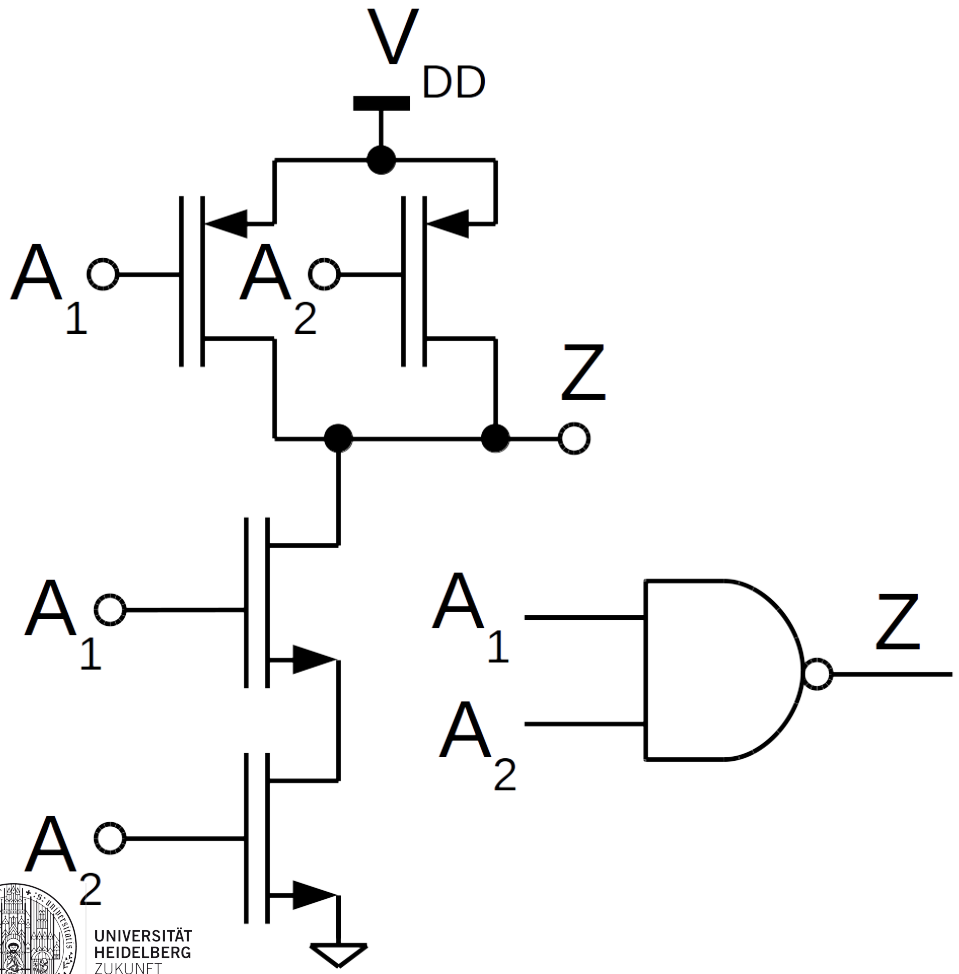




A	Z
0	1
1	0

Combinational logic: NAND gate

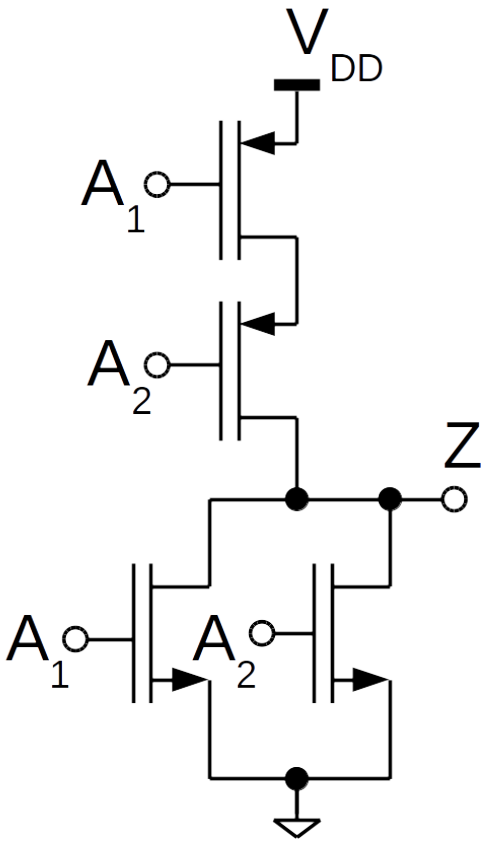
NAND Gate:

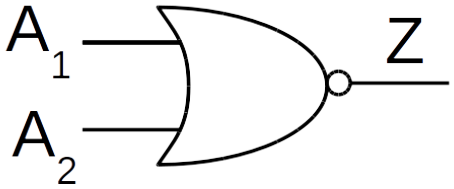


A_1	A_2	Z
0	0	1
0	1	1
1	0	1
1	1	0

Combinational logic: NOR gate

NOR Gate:

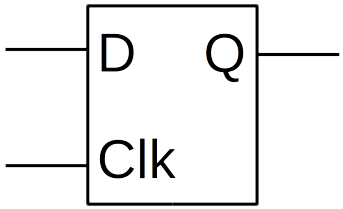


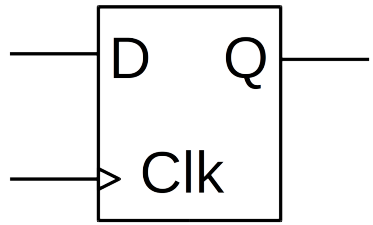


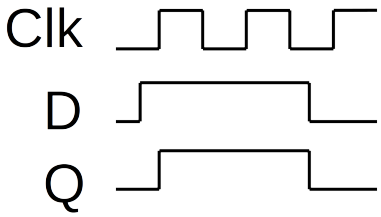
A_1	A_2	**Z**
0	0	1
0	1	0
1	0	0
1	1	0

All other combinational functions can be generated using previous elements.

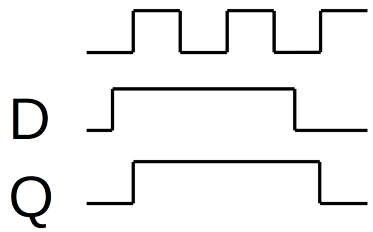
Of course sequential cells can also be used/implemented;







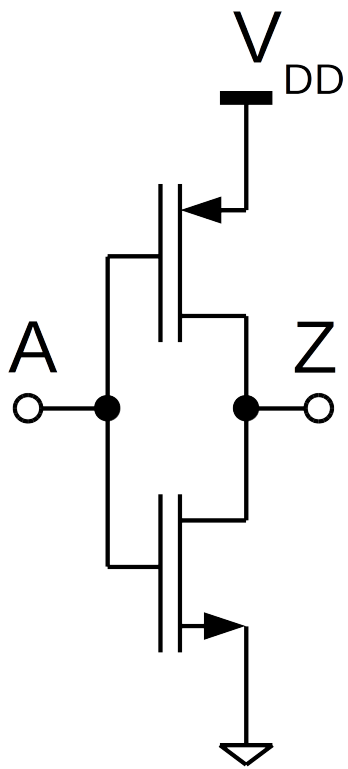
Latch stores data when clock low.

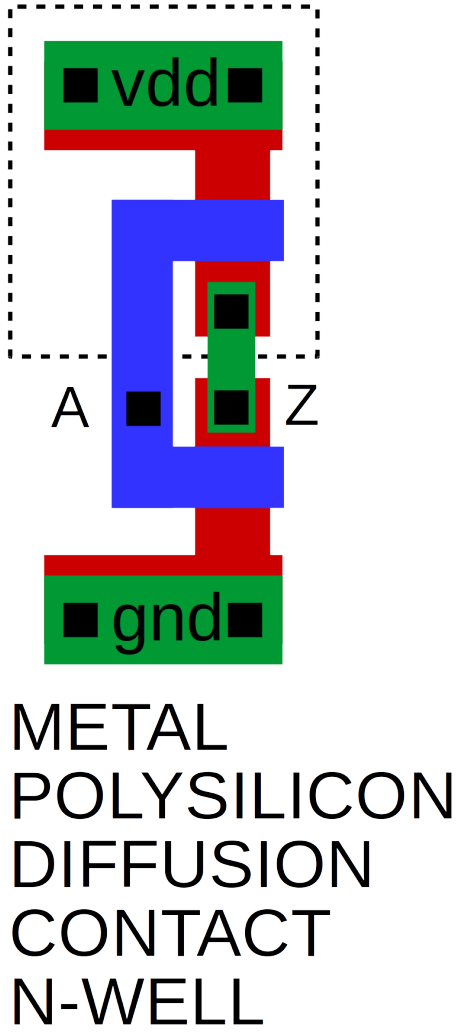


Register stores data when clock rises.

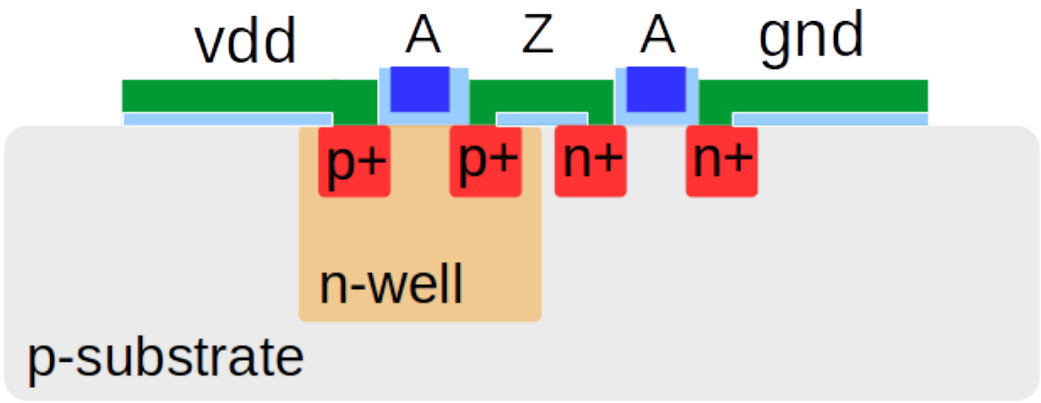
More constrains added, setup/hold time for clocked systems.

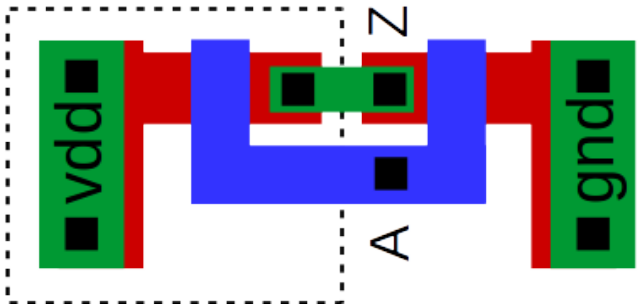
Standard cell example: Inverter

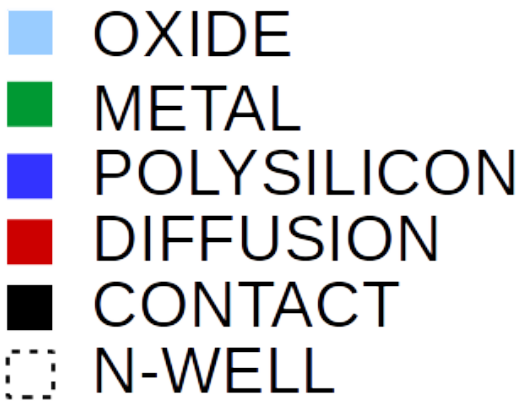




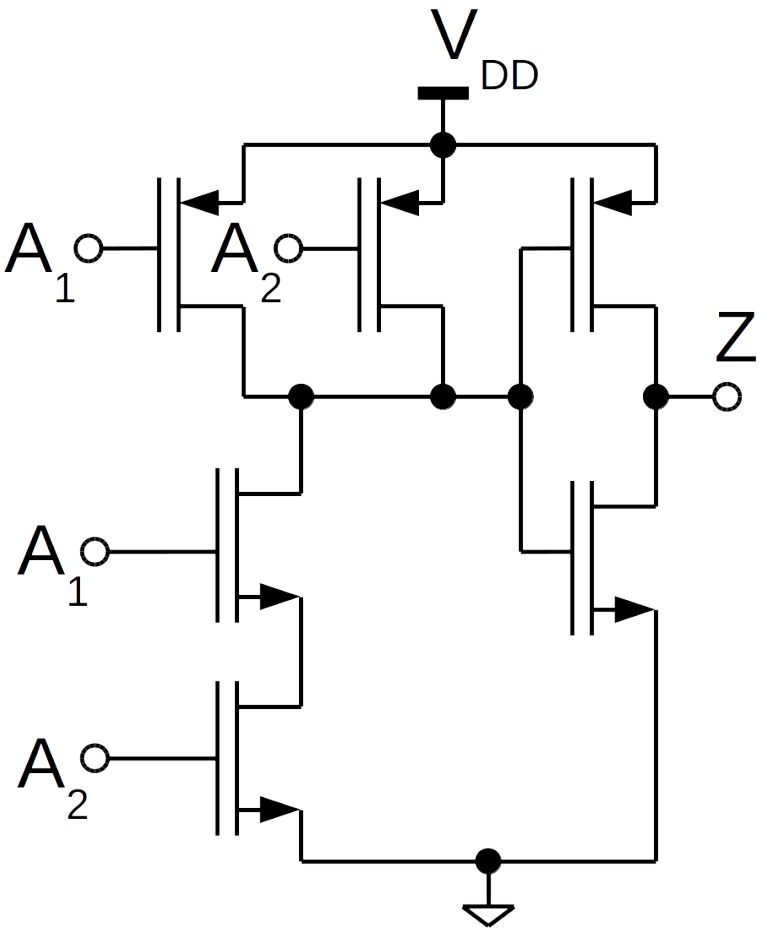
Inverter Cross section

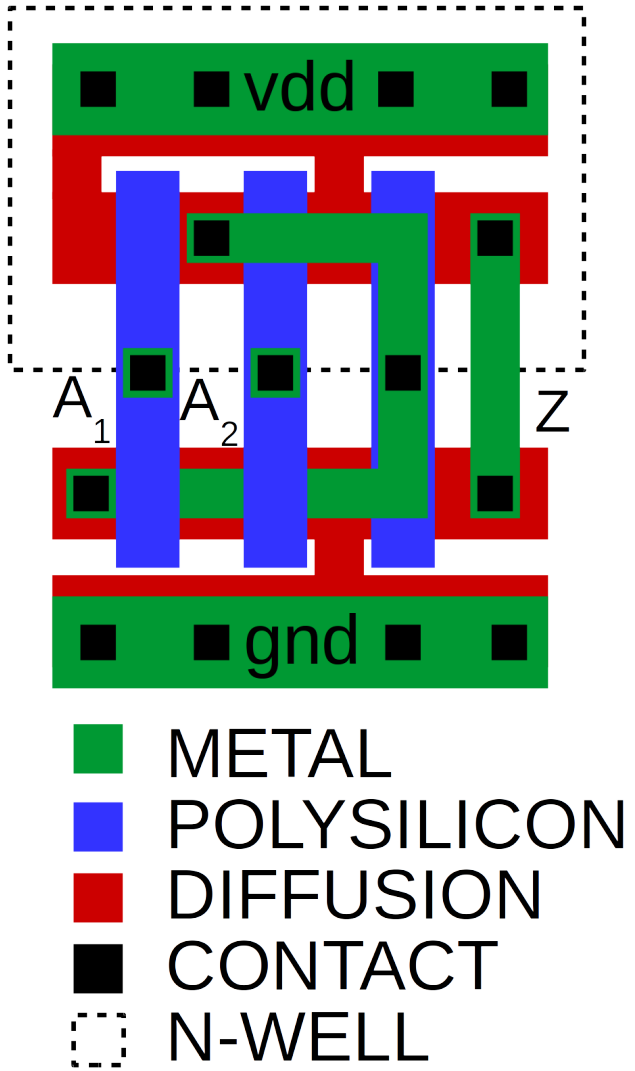






Standard cell example: AND gate

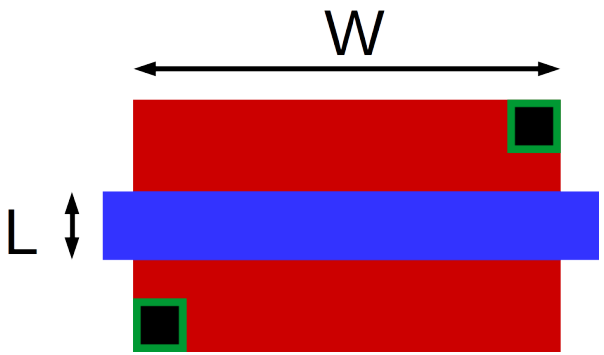


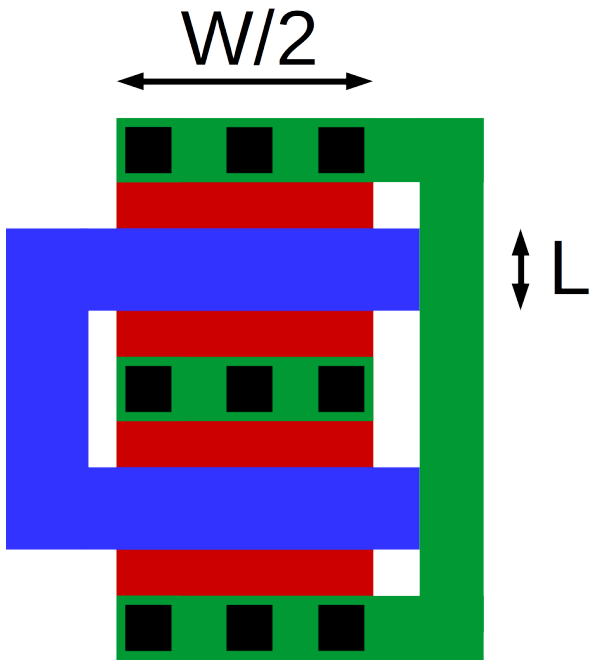


Layout of Standard cells

- Transistors use minimum Length usually.
- Effective R scales linearly with 1/W.
- Gate capacitance scales linearly with W.
- Diffusion capacitance scales linearly with W.

Some recommendation for long transistors:

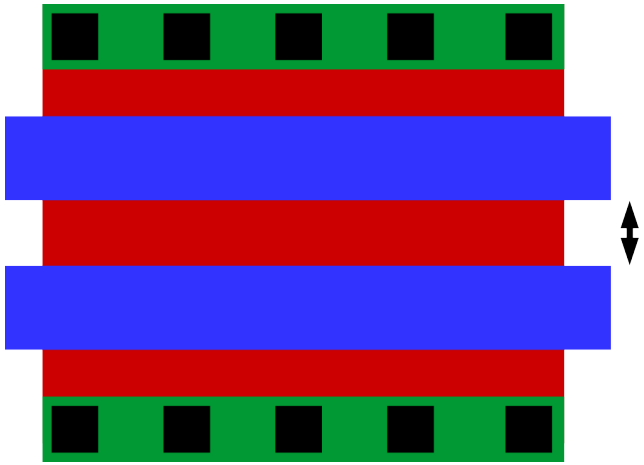


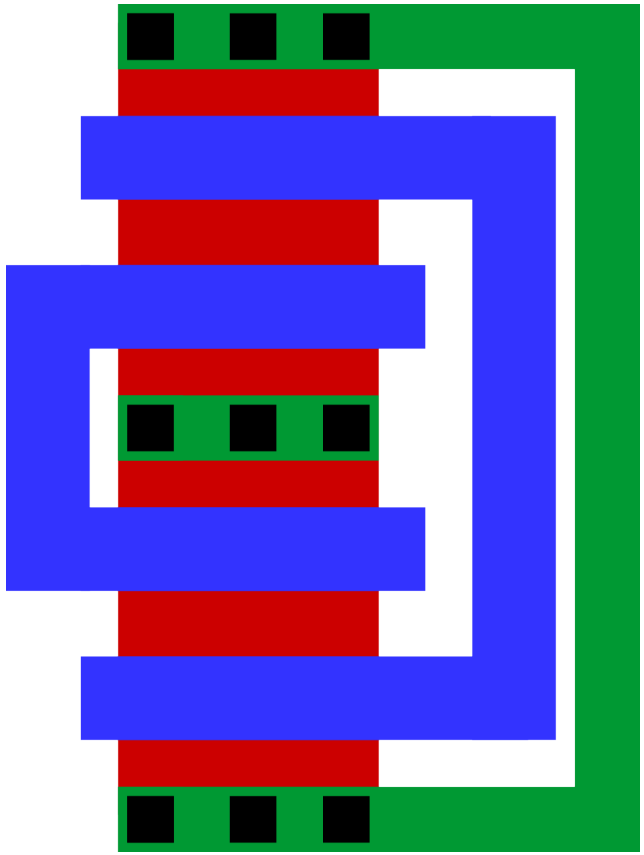


- Long transistors have large diffusion C.
- Folded reduces diffusion C,

Layout of Standard cells

Some recommendation for long transistors:

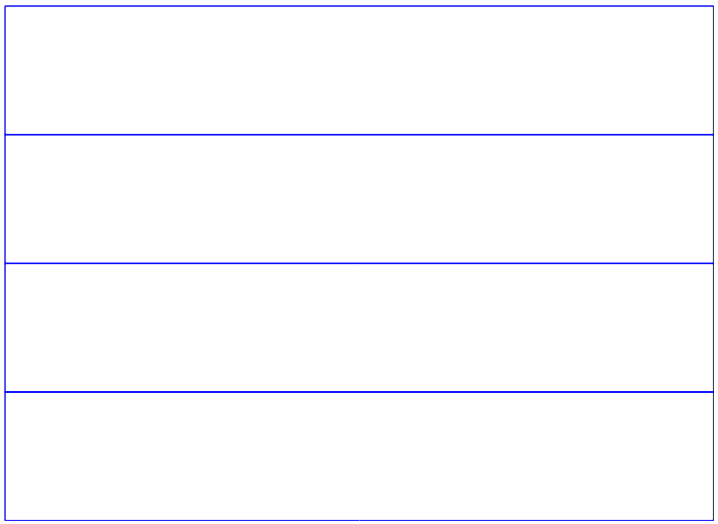




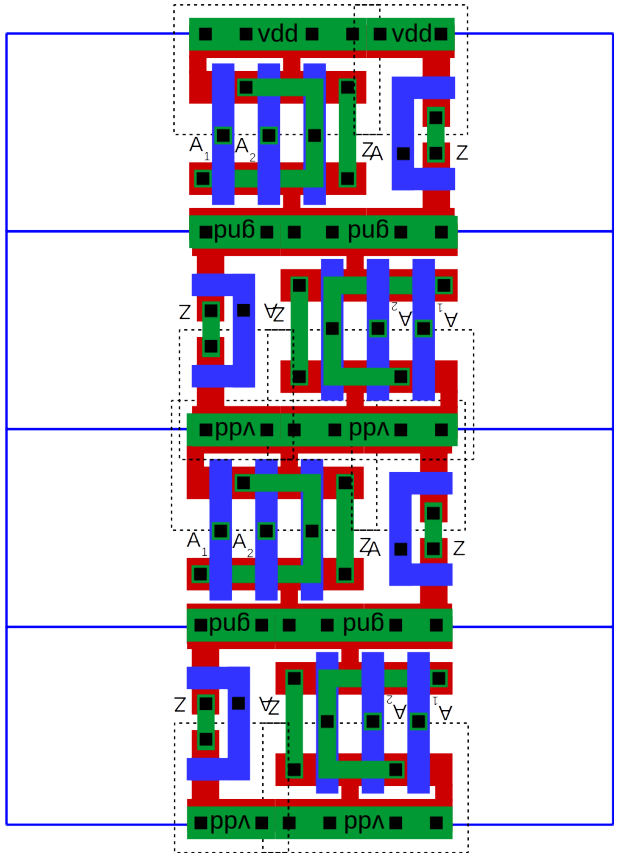
- Series transisors as close as possible reduce R and C parasitics.
- Folded stack not individual transistors.

Place and route

- Digital tools start with defining a grid for placement;



- Cells are placed at each row with interleaved rotation.
- Metals are routed in horizontal and vertical directions.



Modern standard cells

- Modern technologies provide different "flavours" of standard cells.
- They can be combined by synthesis tools depending on constrains.
- Use of different types of transistors;
  - Regular-Voltage-Threshold (STD)
    - Used as default/reference.
  - High-Voltage-Threshold (HVT)
    - Slower.
    - Less power consumption.
  - Low-Voltage-Threshold (LVT)
    - Faster.
    - More power consumption.

Exercise 1: Standard cells design

Design an AND gate with following requirements;

- Same rising/falling time.
- Driving power $= 1$ (an inverter must be designed also).
- Minimum size as possible.

Are the rising/falling times equal in MonteCarlo?
Can you fit it in $3\mu m$ height?